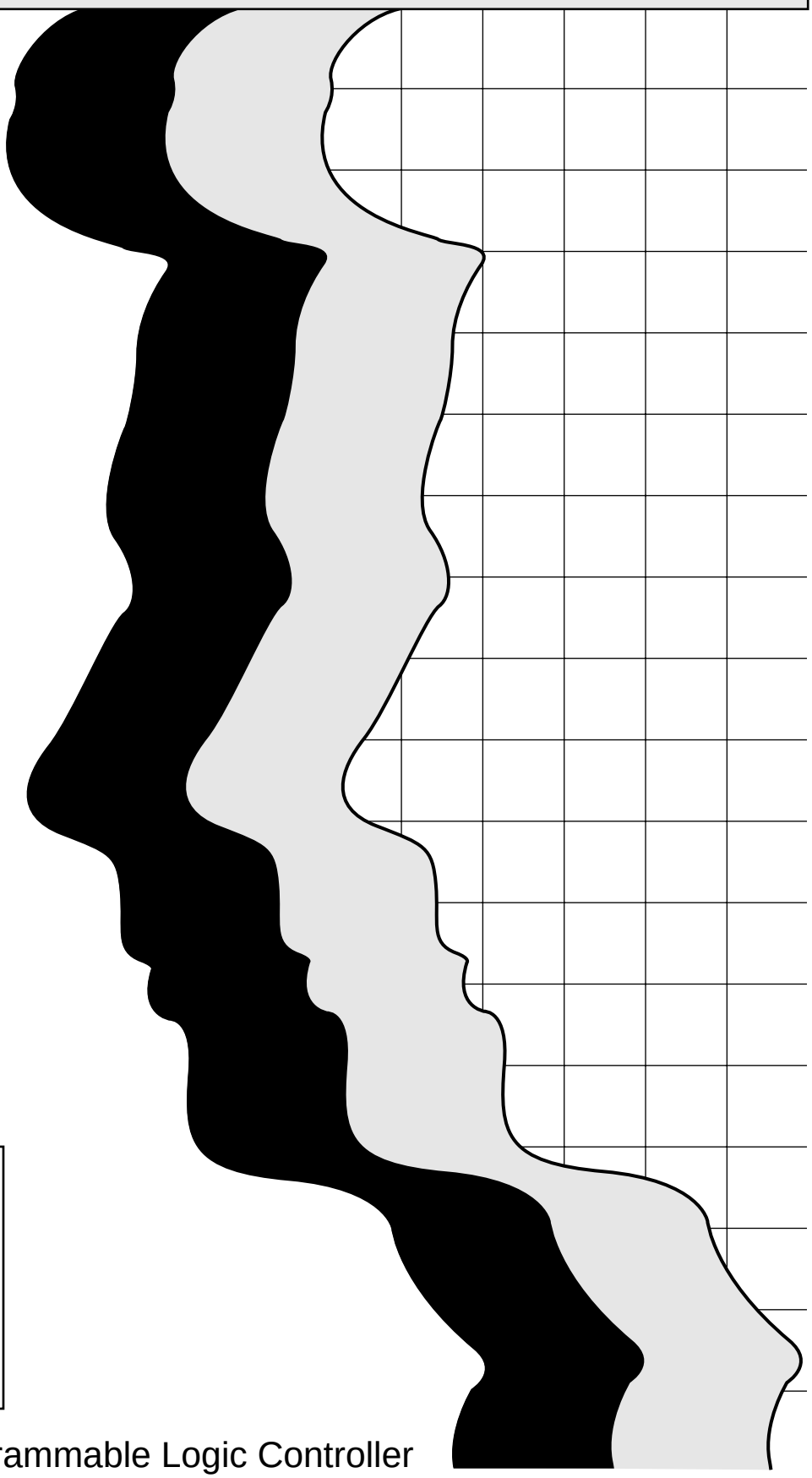
MITSUBISHI

Digital-Analog Converter Module
Type A616DAV

User's Manual



MELSEC

Mitsubishi Programmable Logic Controller

● SAFETY PRECAUTIONS ●

(Always read these instructions before using this equipment.)

Before using this product, please read this manual and the relevant manuals introduced in this manual carefully and pay full attention to safety to handle the product correctly.
The instructions given in this manual are concerned with this product. Refer to the User's Manual of the CPU module in use for details on the safety instructions for the programmable logic controller system.
In this manual, the safety instructions are ranked as "DANGER" and "CAUTION".

⚠ DANGER	Indicates that incorredt handling may cause hazardous conditions, resulting in death or severe injury.
⚠ CAUTION	Indicates that incorredt handling may cause hazardous conditions, resulting in medium or slight personal injury or physical damage.

Note that the ⚠ **CAUTION** level may lead to a serious consequence according to the circumstances. Always follow the instructions of both levels because they are important to personal safety.

Please save this manual to make it accessible when required and always forward it to the end user.

[DESIGN PRECAUTIONS]

⚠ DANGER

- Install a safety circuit external to the PLC that keeps the entire system safe even when there are problems with the external power supply or the PLC module.
  Otherwise, trouble could result from erroneous output or erroneous operation.
  (1) The analog output state will differ according to the setting state of the various functions for controlling the analog output.
  Take special care when making the settings.
  Refer to section 3.3 for details on the analog output state.
  (2) If there is a fault in the output element or the internal circuit, correct outputs may not be possible or erroneous outputs may be made.
  Provide a circuit to externally monitor output signals that could lead to major faults.
- When DC±15V power is supplied externally, make so that this is a system that will simultaneously be turned on and off with the A616DA system. If the power for the A616DA system is turned on/off while external power is being supplied, the erroneous output could cause an accident.

⚠ CAUTION

- Do not bunch the control wires or conmmunication cables with the main circuit or power wires, or install them close to each other.
  They should be installed 100mm (3.94inch) or more from each other.
  Not doing so could result in noise that would cause erroneous operation.
- At power ON/OFF, voltage or current may instantaneously be output from the output terminal of this module.
  In such case, wait until the analog output becomes stable to start controlling the external device.

[INSTALLATION PRECAUTIONS]

⚠CAUTION

- Use the PLC in an environment that meets the general specifications give in the User's Manual of the CPU module in use.
  Using this PLC in an environment outside the range of the general specifications could result in electric shock, fire, erroneous operation, and damage to or deteriouation of the product.
- Securely insert the module fixing latch on the module bottom into the fixing holes on the base unit before mounting. Incorrect mounting of the module could lead to erroneous operation, faults or drop.
- Do not directly touch the module's conductive parts or electronic components.
  Touching the conductive parts could cause an operation failure or give damage to the module.

[WIRING PRECAUTIONS]

⚠CAUTION

- Always ground the FG terminal for the PLC.
  There is a risk of malfunction.
- When wiring in the PLC, be sure that it is done correctly by checking the product's rated voltage and the terminal layout.
  Connecting a power supply that is different form the rating or incorrectly wiring the product could result in fire or damage.
- Tighten the terminal screws with the specified torque.
  If the terminal screws are loose, it could result in short circuits, fire, or erroneous operation.
- Be sure there are no foreign substances such as sawdust or wiring debris inside the module.
  Such debris could cause fires, damage, or erroneous operation.

[STARTUP AND MAINTENANCE PRECAUTIONS]

⚠DANGER

- Externally shut off all power phases before touching the terminals.
  Failure to observe this could lead to erroneous operation.
- Be sure to shut off all phases of the external power supply before cleaning or retightening the terminal screws.
  Not doing so could result in erroneous operation.

⚠CAUTION

- Do not disassemble or modify the module.
  Doing so could cause trouble, erroneous operation, injury, or fire.
- Be sure to shut off all phases of the external power supply used by the system before mounting or removing the module.
  If you do not switch off the external power supply, it will cause failure or malfunction of the module.
- Before handling the module, always touch grounded metal, etc. to discharge static electricity from the human body.
  Failure to do so can cause the module to fail or malfunction.

[DISPOSAL PRECAUTIONS]

⚠CAUTION

- When disposing of the product, handle it as industrial waste.

REVISIONS

※The manual number is given on the bottom left of the back cover.

Print Date	*Manual Number	Revision
Mar., 1989	IB (NA) 66172-A	First edition
Apr., 2001	IB (NA) 66172-B	Addition SAFETY PRECAUTIONS, WARRANTY Correction Section 1.2, 2.1.1, 2.2, 2.3, 3.1, 3.2, 3.3, 3.4.2, 4.1, 4.2, 4.5, 4.6.2, 5.1, 5.2.2, 5.4.1, 5.4.3, 6.4, Appendix 2.1, 2.2, 3.1, 3.2.1, 3.2.3
Nov., 2004	IB (NA) 66172-C	Addition Chapter 5 Correction SAFETY PRECAUTIONS, Section 3.1, 4.2, 5.3.5, WARRANTY

INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end User.

CONTENTS

Conformation to the EMC Directive and Low Voltage Instruction

For details on making Mitsubishi PLC conform to the EMC directive and low voltage instruction when installing it in your product, please see Chapter 3, "EMC Directive and Low Voltage Instruction" of the User's Manual (Hardware) of the PLC CPU to use.

The CE logo is printed on the rating plate on the main body of the PLC that conforms to the EMC directive and low voltage instruction.

By making this product conform to the EMC directive and low voltage instruction, it is not necessary to make those steps individually.

MEMO

1. INTRODUCTION

This manual gives specifications, handling, programming and other information on the A616DAV digital-to-analog converter module (referred to as "A616DA") for use with a MELSEC-A series CPU module.

The A616DA allows a 16-bit signed binary (data part: 12 bits) value defined from the ACPU to be converted into a "−10V to 0V to +10V" or "−5V to 0V to +5V" voltage and to be output to 16 external devices.

1.1 Features

(1) Allows digital-to-analog conversion for 16 channels.

The A616DA can output analog values (voltage) to 16 external devices. (The channels are non-isolated.)

(2) Allows the output voltage range to be specified per channel.

A jumper allows the output voltage range to be set to "−10V to 0V to +10V" or "−5V to 0V to −5V" for each channel.

(3) Allows D/A conversion to be enabled/disabled per channel.

D/A conversion can be performed for only used channels by disabling unused channels for D/A conversion in the sequence program.

(4) Allows analog output to be enabled/disabled on a channel basis.

Analog value output can be enabled or disabled for each channel by the sequence program.
The channel disabled for analog output provides an analog output value of 0V.

(5) Allows analog output to be held (for all channels) at STOP of ACPU.

A jumper allows analog output to be held or not held when the ACPU stops.

(6) Allows offset/gain adjustment to be made without potentiometers.

The offset and gain values can be specified by the UP/DOWN switch for each channel.

1.2 Generic Names of CPUs

The three generic CPU names used in this manual include the following CPU types:

(1) Building block type CPU

A1CPU(P21/R21)
A2CPU(P21/R21)
A2CPU-S1(P21/R21)
A3CPU(P21/R21)
A1NCPU(P21/R21)
A2NCPU(P21/R21)
A2NCPU-S1(P21/R21)
A3NCPU(P21/R21)
A3HCPU(P21/R21)
A2ACPU(P21/R21)
A2ACPU-S1(P21/R21)
A3ACPU(P21/R21)
A2UCPU
A2UCPU-S1
A3UCPU
A4UCPU
A73CPU(P21/R21)
A3MCPU(P21/R21)
A81CPU
Q2ACPU
Q2ACPU-S1
Q3ACPU
Q4ACPU
Q4ARCPU

(2) Small-type building block type CPU

A1SCPU(S1)
A1SJCPU(S3)
A2ASCPU(S1/S30)
A1SJHCPU(S8)
A1SCPUC24-R2
A1SHCPU
A2SCPU(S1)
A2SHCPU(S1)
A2USHCPU-S1
Q2ASCPU(S1)
Q2ASHCPU(S1)

(3) Compact-type CPU

A0J2CPU(P23/R23)
A0J2HCPU(P21/R21)
A52GCPU(T21B)

2. SYSTEM CONFIGURATION

2.1 Overall Configuration

2.1.1 Building block type CPU system

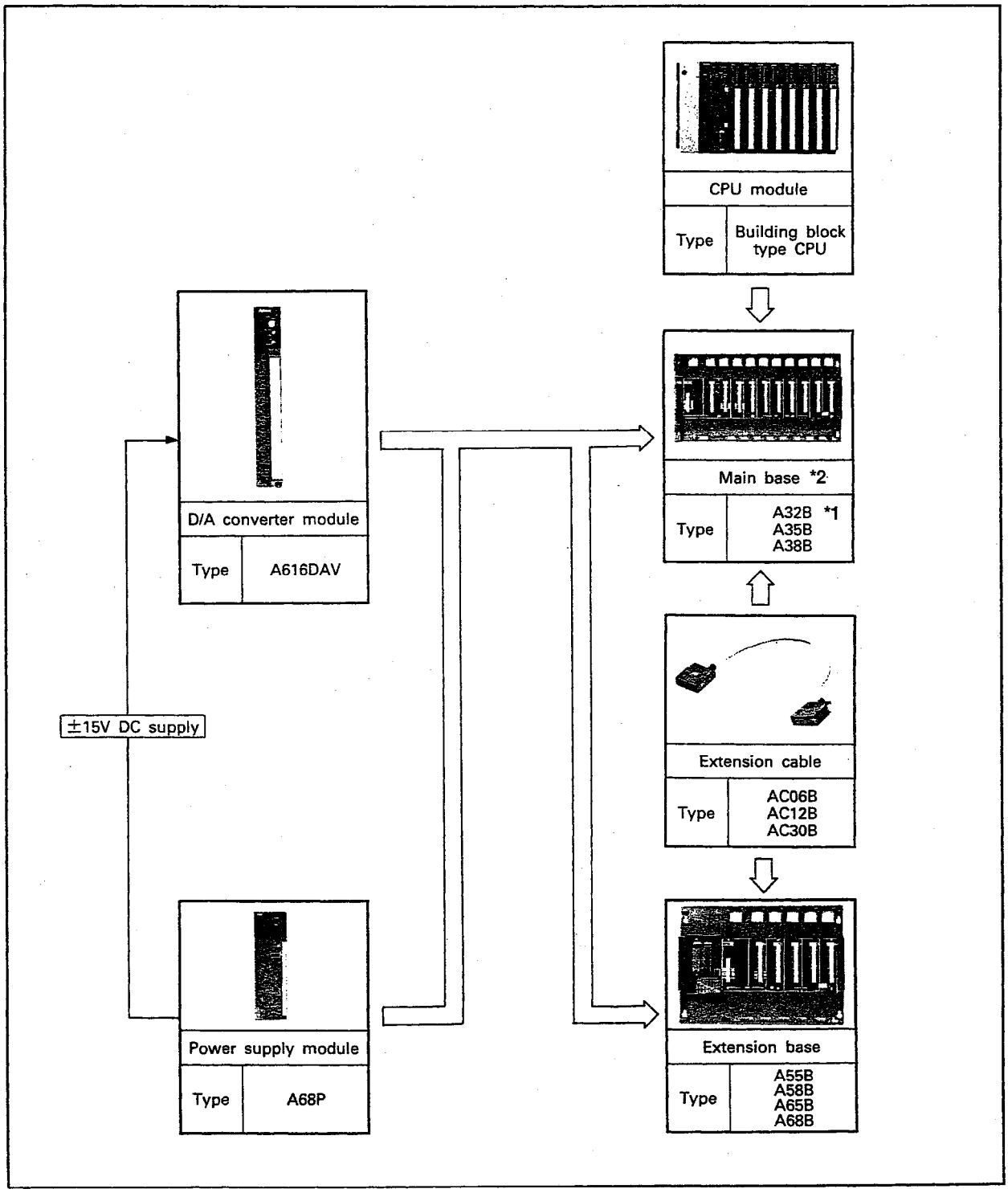


Fig. 2.1 Building Block Type CPU System Configuration

REMARKS

1) *1····· An extension base cannot be connected to the A32B.
2) *2····· When using the A73CPU,A81CPU, the basic base will be the following.
   - A73CPU : A74B (A616DAV cannot be used with A74B)
   - A81CPU : A78B (Expansion base cannot be connected.)

2.1.2 Compact type CPU system

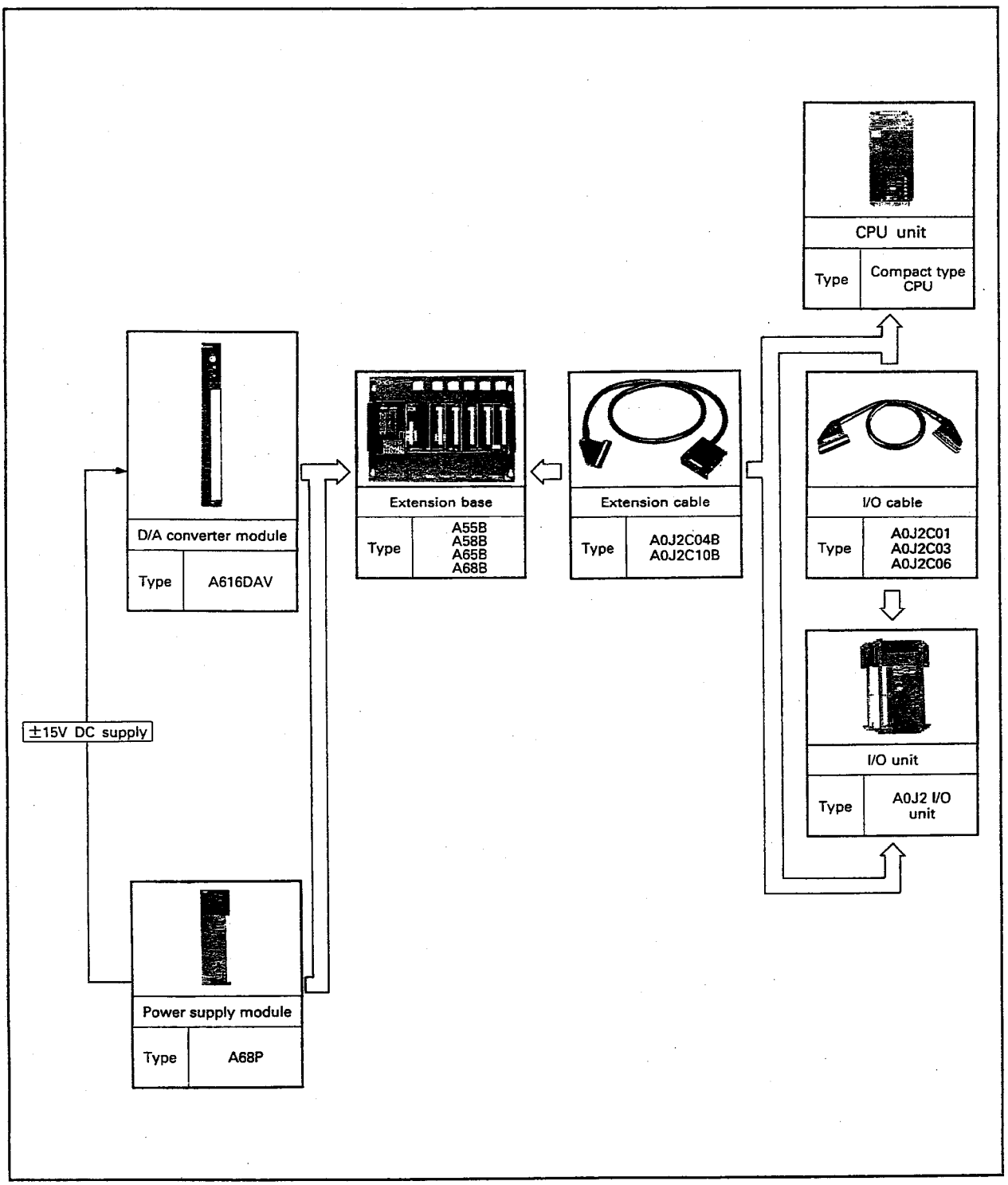


Fig. 2.2 Compact Type CPU System Configuration

2.2 Applicable A-Series Systems

(1) The A616DA can be used with the following CPU modules:

Applicable models		
A0J2CPU	A3UCPU	A1SJCPU(S3)
A0J2HCPU	A4UCPU	A1SJHCPU(S8)
A1NCPU	A73CPU	A1SCPU(S1)
A2NCPU	A81CPU	A1SCPUC24-R2
A2NCPU-S1	A1CPU	A1SHCPU
A3NCPU	A2CPU	A2SCPU(S1)
A3HCPU	A2CPU-S1	A2SHCPU(S1)
A3MCPU	A3CPU	A2ASCPU(S1/S30)
A2ACPU	Q2ACPU	A2USHCPU-S1
A2ACPU-S1	Q2ACPU-S1	Q2ASCPU(S1)
A3ACPU	Q3ACPU	Q2ASHCPU(S1)
A2UCPU	Q4ACPU	A52GCPU
A2UCPU-S1	Q4ARCPU	

(2) The number of A616DAs used is unlimited if within the range of the I/O points of the CPU module used.

(3) The A616DA may be loaded into any slot on the base unit with the following precautions:

(a) When using the A616DA with the A55B or A58B extension bases (i.e. those without power supplies), select the power supply for the main base unit in accordance with the relevant CPU module User's Manual.

(b) When used with the A3CPU(P21/R21), the A616DA cannot be loaded in the last slot of the 7th extension stage in a system for which I/O allocation has been made or link X, Y defined in the parameters.
(These restriction is not applied for A3NCPU, A3HCPU, A3MCPU, A73CPU, A3ACPU.)

(4) On a data link system, the A616DA can be mounted to any of the following: master station, local station or remote I/O.
Refer to the MELSECNET、MELSECNET/B data link system reference manual for examples of programs for remote I/O stations.

POINT

(1) The A616DA cannot be used in an A0J2P25/R25 (remote I/O station).

2.3 Notes on Configuring the System

When using the A616DA, an external power supply is required to supply ±15V DC to the A616DA.

(a) The MELSEC-A series A68P power supply module for use on a base unit is available as a ±15V DC power supply. (For full information, see Appendix 3.)

(b) If the A68P power supply module is not used, the power supply used must conform to the specifications given in Section 3.7. In this case, it is recommended to use noise filters with the A616DA. (See Section 4.6.3.)

(c) With DC ±15V, make so that this is a system that will simultaneously be turned on and off with the A616DA system.

3. SPECIFICATIONS

Gives general specifications, A616DA performance specifications, I/O conversion characteristics, etc.

3.1 General Specifications

Table 3.1 shows the common specifications of various units used.

Item	Specifications					
Operating ambient temperature	0 to 55℃					
Storage ambient temperature	-20 to 75℃					
Operating ambient humidity	10 to 90%RH, non-condensing					
Storage ambient humidity	10 to 90%RH, non-condensing					
Vibration resistance	Conforming to JIS B 3502, IEC 61131-2		Frequency	Acceleration	Amplitude	Sweep count
		Under intermittent vibration	10 to 57 Hz	———	0.075 mm (0.003 in.)	10 times each in X, Y, Z directions (for 80 min.)
			57 to 150 Hz	9.8m/s²	———	
		Under continuous vibration	10 to 57 Hz	———	0.035 mm (0.001 in.)	
			57 to 150 Hz	4.9m/s²	———	
Shock resistance	Conforming to JIS B 3502, IEC 61131-2 (147m/s², 3 times each in X, Y, Z directions)					
Noise durability	By noise simulator of 1500Vpp noise voltage, 1μs noise width and 25 to 60Hz noise frequency					
Dielectric withstand voltage	1500V AC for 1 minute across AC external terminals and ground 500V AC for 1 minute across DC external terminals and ground					
Insulation resistance	5MΩ or larger by 500V DC insulation resistance tester across AC external terminals and ground					
Grounding	Grounding is required; it is not required when it is impossible.					
Operating ambiance	No corrosive gas					
Operating height *3	2000 m (6562 ft.) max.					
Installation location	Inside the control panel					
Overvoltage categry *1	II or less					
Pollution rate *2	2 or less					
Cooling method	Self-cooling					

Table 3.1 General Specifications

*1: Indicates the distribution area where the device is assumed to be connected, from the public power distribution network to the local machine device.
Category II is applied to the devices to which the power is supplied from a fixed equipment.
The surge resistace voltage of a rated 300 V device is 2500 V.

*2: This is an index which Indicates the occurrence rate of the conductive object in the anvironment where the device is used.
Pollution rate II indicates that only non-conductive pollution may occur with a possiblity of generating temporary conductivity due to accidental condensation.

*3: Do not use or store the PLC under pressure higher than the atmospheric pressure of altitude 0m.
Doing so can cause a malfunction.
When using the PLC under pressure, please contact your sales representative.

3.2 Performance Specifications

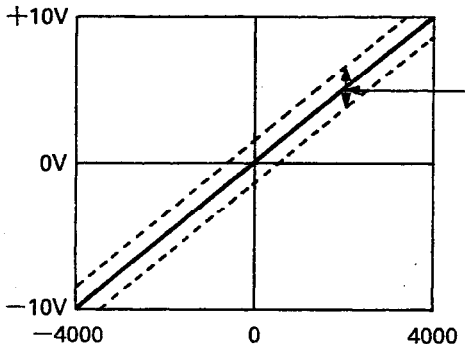
<table>
<tr><th colspan="2">Item</th><th colspan="2">Specifications</th><th>Relevant Section</th></tr>
<tr><td colspan="2">Digital input
(ACPU to A616DA)</td><td colspan="2">1) 16-bit signed binary (data part: 12 bits)
2) Setting range: −4096 to 4095</td><td>———</td></tr>
<tr><td colspan="2">Analog output
(A616SA to external device)</td><td colspan="2">1) −10V to 0V to +10V when output voltage range setting is 10V.
(External load resistance: 2KΩ to 1MΩ)
1) −5V to 0V to +5V when output voltage range setting is 5V.
(External load resistance: 2KΩ to 1MΩ)</td><td>———</td></tr>
<tr><td colspan="2">I/O characteristics</td><td colspan="2"><table><tr><th rowspan="2">Digital input</th><th colspan="2">Analog output</th></tr><tr><th>5V setting</th><th>10V setting</th></tr><tr><td>+4000</td><td>+5.0V</td><td>+10V</td></tr><tr><td>+2000</td><td>+2.5V</td><td>+5V</td></tr><tr><td>0</td><td>0V</td><td>0V</td></tr><tr><td>−2000</td><td>−2.5V</td><td>−5V</td></tr><tr><td>−4000</td><td>−5.0V</td><td>−10V</td></tr></table></td><td>Section 3.4</td></tr>
<tr><td colspan="2">Digital value resolution</td><td colspan="2">1/4000</td><td>———</td></tr>
<tr><td colspan="2">Voltage range setting</td><td>10V</td><td>5V</td><td rowspan="3">———</td></tr>
<tr><td rowspan="2">Overall accuracy (%)</td><td>ambient temperature (0~55℃)</td><td>±0.6%(±60mV)</td><td>±0.6%(±30mV)</td></tr>
<tr><td>ambient temperature (25℃)</td><td>±0.3%(±30mV)</td><td>±0.3%(±15mV)</td></tr>
<tr><td colspan="2">Sampling period (ms)</td><td colspan="2">1.5 + 0.5 × (number of D/A conversion enable channels)</td><td>Section 3.5.1</td></tr>
<tr><td colspan="2">Conversion speed (ms)</td><td colspan="2">0.5 (time requined for conversion from −10V to +10/+10V to)−10V)</td><td>Section 3.5.2</td></tr>
<tr><td colspan="2">Absolute maximum output (V)</td><td colspan="2">15</td><td>———</td></tr>
<tr><td colspan="2">Number of analog output channels</td><td colspan="2">16 channels/module</td><td>———</td></tr>
<tr><td colspan="2">Isolation</td><td colspan="2">1) Photocoupler isolated between output terminals and PLC power supply.
2) Non-isolated between A616DA channels.</td><td>———</td></tr>
<tr><td colspan="2">Number of I/O points</td><td colspan="2">32</td><td>———</td></tr>
<tr><td colspan="2">Terminals</td><td colspan="2">38-point terminal block</td><td>———</td></tr>
<tr><td colspan="2">Wire size (mm²)</td><td colspan="2">0.75 to 2 (18 to 14 AWG)</td><td>———</td></tr>
<tr><td colspan="2">Solderless terminal</td><td colspan="2">V1.25-3, V1.25-YS3A, V2-S3, V2-YS3A</td><td>———</td></tr>
<tr><td colspan="2">Internal current consumption (5V DC) (A)</td><td colspan="2">0.38</td><td>———</td></tr>
<tr><td rowspan="2">External supply power*</td><td>Voltage</td><td colspan="2">+15V DC/−15V DC</td><td rowspan="2">Section 3.7</td></tr>
<tr><td>Current</td><td colspan="2">0.2A for +15V DC/0.17V for −15V DC</td></tr>
<tr><td colspan="2">External dimensions mm(inch)</td><td colspan="2">250(9.84) × 37.5(1.48) × 131(5.16)</td><td>———</td></tr>
<tr><td colspan="2">Weight kg</td><td colspan="2">0.65</td><td>———</td></tr>
</table>

Table 3.2 Performance Specifications

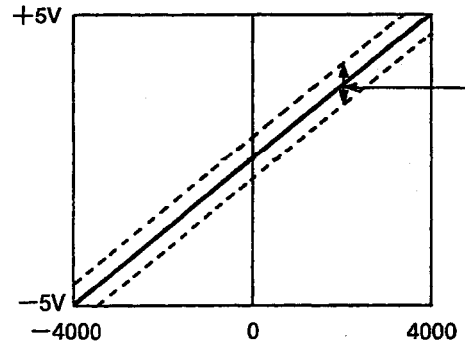
REMARKS

1) Overall accuracy

Accuracy in reference to the value (10V/5V) set by the output voltage range setting jumper. The following graph assumes the output voltage range setteing of 10V.



The following graph assumes the output voltage range setting of 5V.



2) * ····· One A68P power supply module can supply ±15V DC to four A616DAs.
(See Appendix 3 for full information on the A68P power supply module.)

3.3 Analog Output Control Functions

(1) Table 3.3 gives various facilities for controlling analog output.

Item	Description	Setting Method
Analog output HOLD/CLEAR setting (for all 16 channels)	(1) Using the jumper, specify whether the analog output at the time of STOP is held (HOLD) or cleared (CLEAR) when the ACPU is set to STOP by the RUN key switch, etc. (a) CLEAR setting: STOP····· 0V or offset value is output. RUN ····· Digital value specified from the ACPU is converted into an analog value and is output only while the output batch enable flag (Y1B) is on. (b) HOLD setting: STOP····· Analog value at the time of STOP is retained. RUN ····· Digital value specified from the ACPU is converted into an analog value and is output independently of the ON/OFF state of the output batch enable flag (Y1B). (2) When the ACPU stops operation on detection of an error, the analog output value is set to 0V independently of the analog output HOLD/CLEAR setting.	Section 4.4.1
D/A conversion disable channel setting (on a channel basis)	(1) Using the sequence program, specify the channel to be disabled for D/A conversion in order to reduce the sampling period. (All 16 channels are enabled for D/A conversion when the ACPU is powered up or reset.) (a) D/A conversion enable channel ····· Performs D/A conversion of the digital value specified from the ACPU. (b) D/A conversion disable channel ····· Does not perform D/A conversion of the digital value specified from the ACPU.	Section 5.3.2
Analog output disable channel setting (on a channel basis)	(1) Using the sequence program, specify the channel to be disabled for analog value output. (All 16 channels are enabled for analog output when the ACPU is powered up or reset.) (a) Analog output enable channel ····· Outputs the offset value or an analog value converted. (b) Analog output disable channel ····· Outputs 0V.	Section 5.3.3

Table 3.3 Analog Output Control Functions

(2) As indicated in Table 3.4, analog output values depend on the settings of the analog output control functions indicated in Table 3.3.

Setting combination / Execution on status	Analog Output HOLD/CLEAR Setting	CLEAR					HOLD		
	Output batch enable flag (Y1B)	ON			OFF		ON/OFF		
	Analog Output disable channel setting	Enable		Disable	Enable	Disable	Enable		Disable
	D/A conversion disable channel setting	Enable	Disable	Enable/Disable	Enable/Disable	Enable/Disable	Enable	Disable	Enable/Disable
When PLC CPU RUN		D/A conversion value output	Offset value	0V	Offset value	0V	D/A conversion value output	Offset value	0V
When PLC CPU STOP		0V	Offset value	0V	Offset value	0V	Outputs the analog output value preceeding the stop	Offset value	0V
When PLC CPU error occurs		0V							
Remote I/O station link error (when mounted to remote I/O station).		0V							

Table 3.4 Analog Output Values

3.4 I/O Conversion Characteristics

3.4.1 I/O conversion characteristics

(1) I/O conversion characteristics

I/O conversion characteristics are provided to convert a digital value specified from the ACPU into an analog value and are indicated by an inclination connected between an offset value and a gain value.

(2) Offset value and gain value

(a) The offset and gain values are defined as follows:

1) Offset value ···· Voltage output from the A616DA when the digital value specified from the ACPU is 0.

2) Gain value ····· Voltage output from the A616DA when the digital value specified from the ACPU is 4000.

(b) The factory-set offset and gain values are as follows:

1) Offset value ···· 0V
2) Gain value ····· 10V

(c) The offset and gain values may be changed in test mode for each channel.

(3) I/O conversion characteristic example

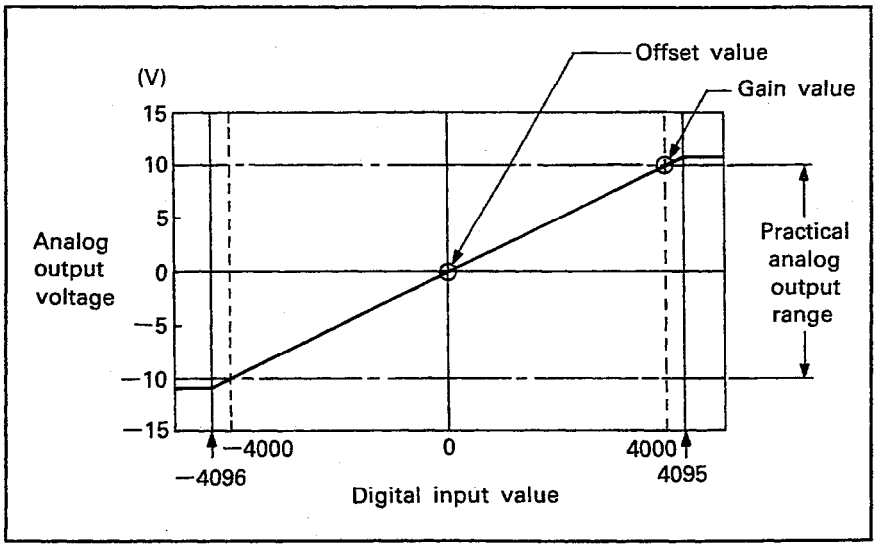


Fig. 3.1 I/O Conversion Characteristic Example

(4) Relation between offset/gain value and analog output

The resolution of the A616DA can be changed as appropriate by the offset/gain value setting.
The analog value resolution and analog output value are calculated by the following equations:

$$\text{(Resolution)} = \frac{\text{(gain value)} - \text{(offset value)}}{4000}$$

$$\begin{aligned}\text{(Analog output)} &= \frac{\text{(gain value)} - \text{(offset value)}}{4000} \\ &\quad \times \text{(digital input value)} + \text{(offset value)} \\ &= \text{(resolution)} \times \text{(digital input value)} \\ &\quad + \text{(offset value)}\end{aligned}$$

As the maximum analog value resolution of the A616DA is as given below, the variation of the analog output value for a change of 1 in the digital input value may not be as calculated above.

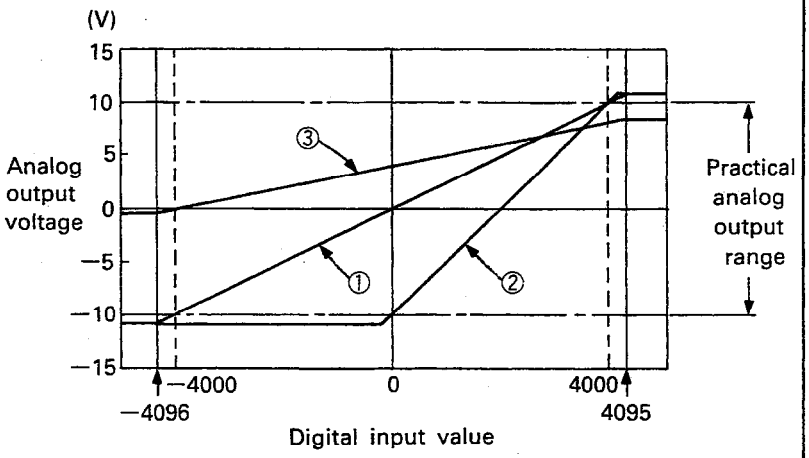
Output Voltage Range Setting	Maximum Resolution
−10V to 0V to +10V	1.3mV
−5V to 0V to +5V	0.65mV

3.4.2 I/O conversion characteristics in response to offset/gain value changes

(1) Offset/gain values vs. I/O conversion characteristics

The relation between the following offset/gain settings and I/O conversion characteristics is shown on the right.

No.	Offset Value	Gain Value
①	0V	+10V
②	−10V	+10V
③	+4V	+8V



Example

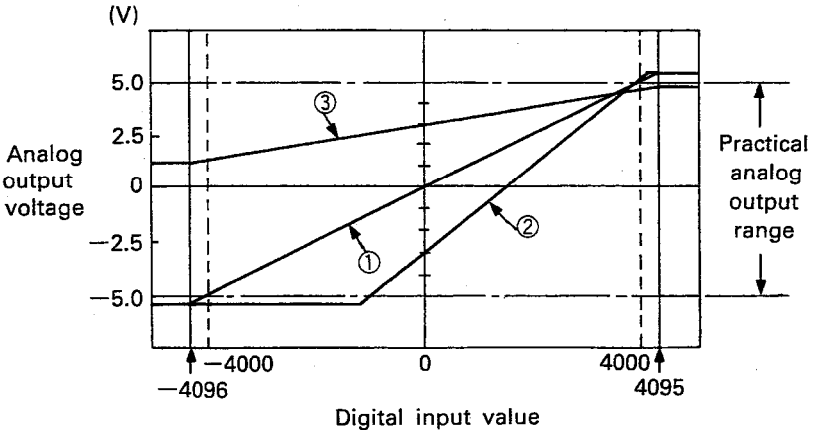
The analog output voltages are as follows at the digital input value settings of 2000 and 500 for the characteristic graphs ① to ③.

No.	Digital Input Value	Analog Output Value
①	2000	+5.0V
	500	+1.25V
②	2000	0V
	500	−7.5V
③	2000	+6.0V
	500	+1.5V

Fig. 3.2 Offset/Gain Values vs. I/O Conversion Characteristics (10V Setting)

The relation between the following offset/gain settings and I/O conversion characteristics is shown on the right.

No.	Offset Value	Gain Value
①	0V	+5.0V
②	−3.0V	+5.0V
③	+3.0V	+4.5V



Example

The analog output voltages are as follows at the digital input value settings of 2000 and −1000 for the characteristic graphs ① to ③.

No.	Digital Input Value	Analog Output Value
①	2000	+2.50V
	−1000	−1.25V
②	2000	+1.00V
	−1000	−5.00V
③	2000	+3.75V
	−1000	+2.63V

Fig. 3.3 Offset/Gain Values vs. I/O Conversion Characteristics (5V Setting)

3.5 D/A Conversion Processing Time

The processing time required for digital-to-analog conversion and output to the external equipment is calculated as follows:

(Processing time) = (sampling period) + (conversion time)

(a) Sampling period
····· Cycle of D/A conversion processing for the same channel.

(b) Conversion speed
····· Time required for the analog value to change to the set value.

3.5.1 Sampling period

(1) The A616DA performs D/A conversion for a D/A conversion enable channel which is switched to another per 0.5ms. A cycle of executing D/A conversion for the same channel is referred to as a sampling period, which is calculated as follows:

$$\text{(Sampling period)} = \underline{1.5} + 0.5 \times \begin{pmatrix}\text{number of D/A conversion}\\ \text{enable channels}\end{pmatrix} \text{ (ms)}$$

(Constant)

(2) The sampling period can be reduced by defining unused channels as channels disabled for D/A conversion.

- Example -

(1) The sampling period is as follows if channels 0 to F (16 channels) are enabled for D/A conversion.

Sampling period = 1.5 + 0.5 × 16 = 9.5 (ms)

(2) The sampling period is as follows if channels 4 to 7 and C to F (8 channels) are disabled for D/A conversion.

Sampling period = 1.5 + 0.5 × 8 = 5.5 (ms)

3.5.2 Conversion speed

(1) Indicates the processing time required for the analog value to change to the specified value after D/A conversion processing.

(2) The maximum coversion speed (−10V to +10V or +10 to −10V) is 0.5ms.

3.6 Function Block Diagram

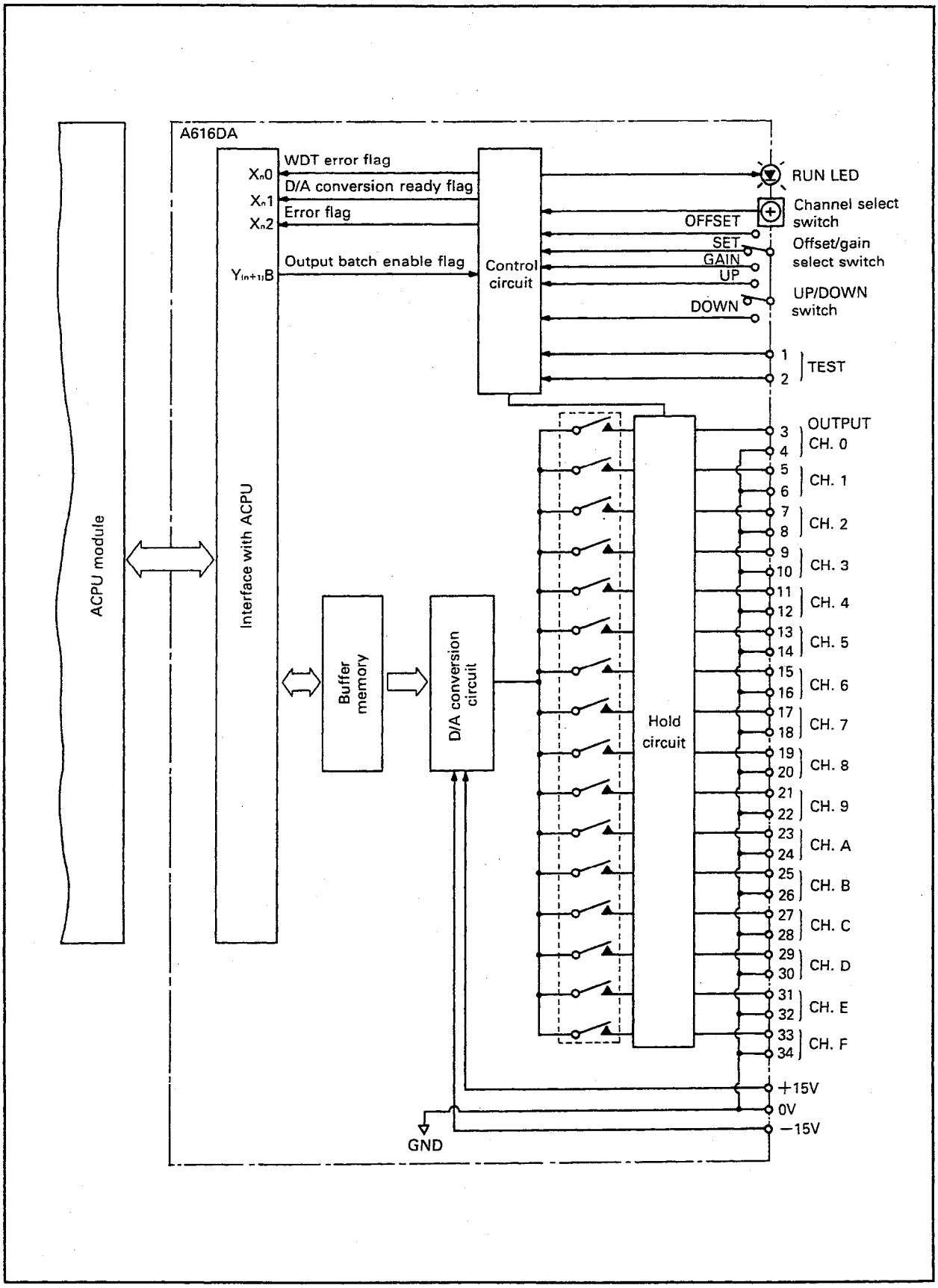


Fig. 3.4 A616DA Function Block Diagram

3.7 External Supply Power (±15V DC) Specifications

The A68P power supply module is recommended for use as a power supply for providing ±15V DC to the A616DA. (Full information on the A68P power supply module is given in Appendix 3.)

When the A68P power supply module is not used, the power supply used to supply ±15V DC to the A616DA must conform to the specifications given in Table 3.5.

Item		Specifications
Voltage		+15V DC ±3% (14.55V to 15.45V)
		−15V DC ±3% (−14.55V to −15.45V)
Current*	+15V DC	0.2A
	−15V DC	0.17A
Ripple voltage		50mVpp max.
Spike voltage		100mVpp max.
Transient output variation		Within ±1V

Table 3.5 External Supply Power (±15V DC) Specifications

REMARKS

1) * ····· The currents indicated in Table 3.5 are those for one A616DA.

4. PRE-OPERATION SETTINGS AND PROCEDURES

4.1 Pre-Operation Procedure

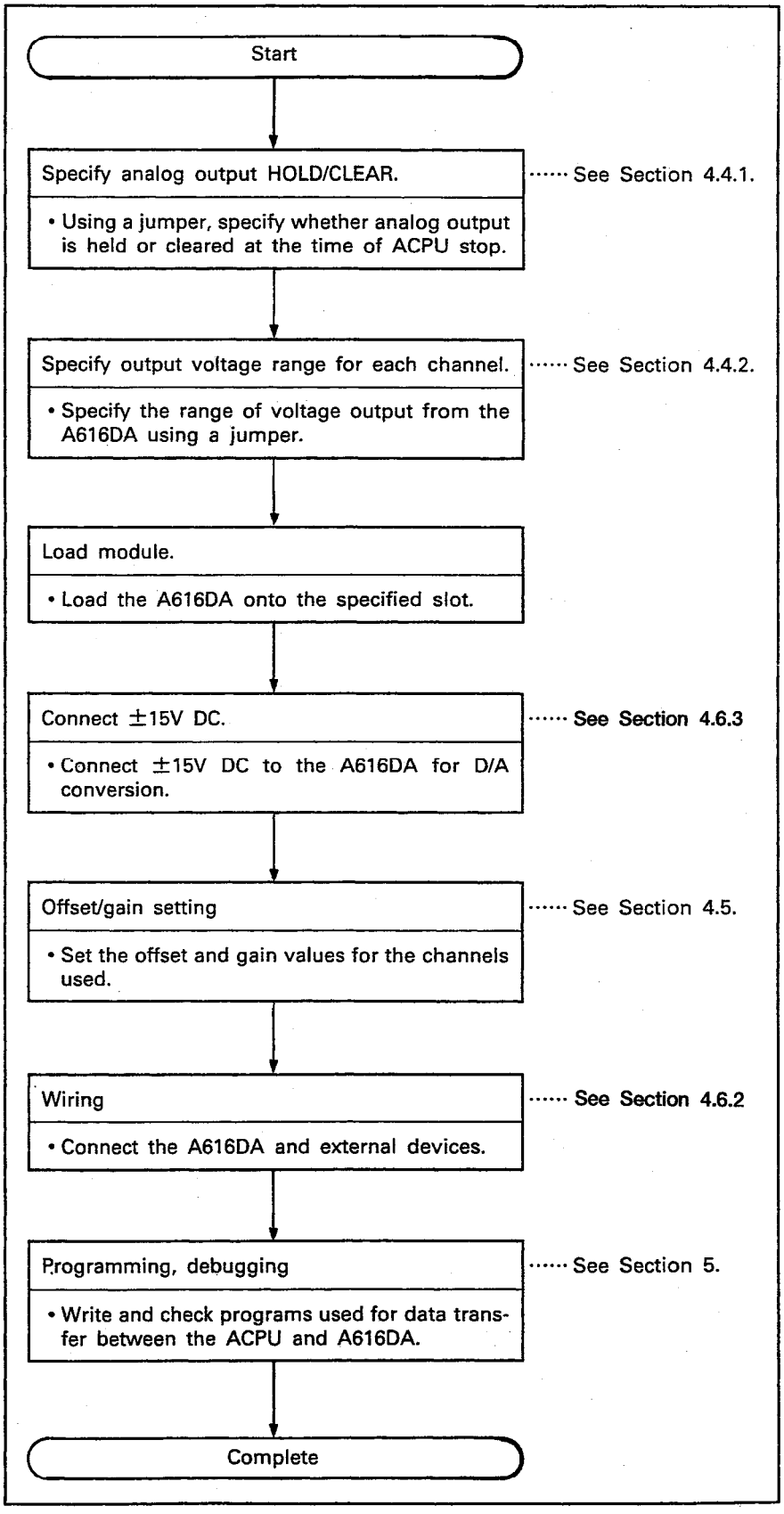


Fig. 4.1 Pre-Operation Procedure

4.2 Handling Instructions

(1) Protect the A616DA and its terminal block from impact loads.

(2) Do not remove the printed circuit boards from the housing. There are no user-serviceable parts on the boards.

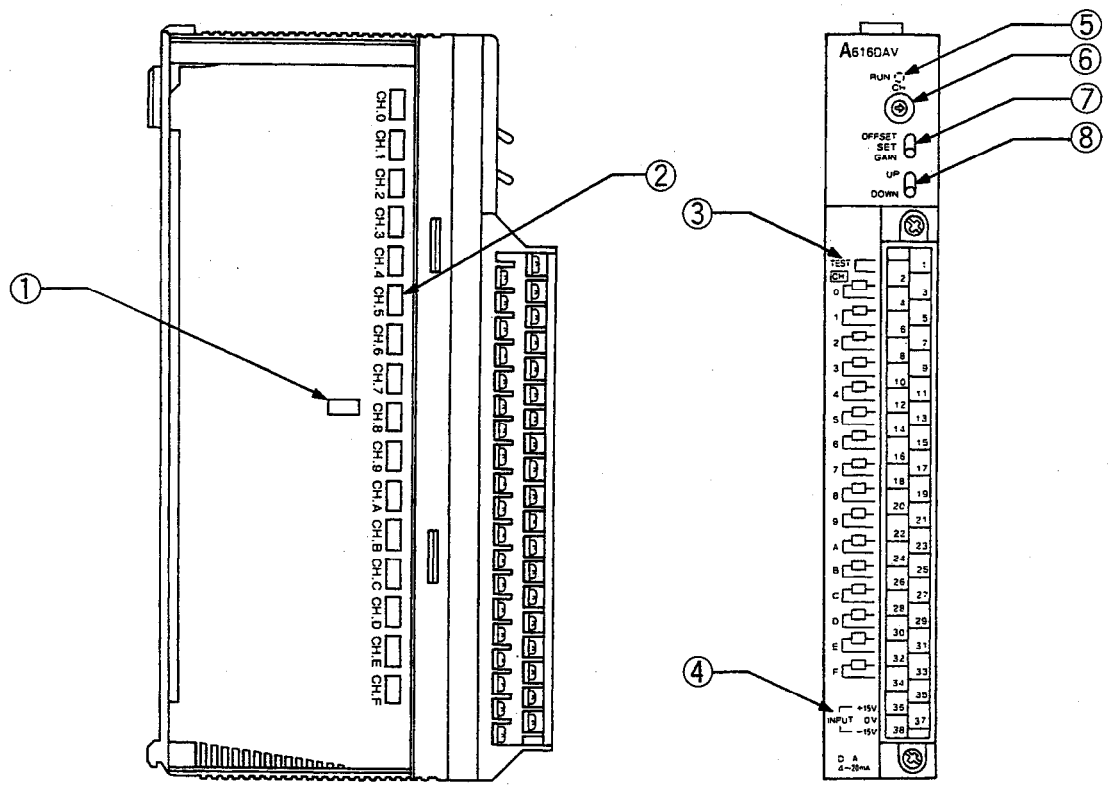
(3) Ensure that no conductive debris can enter the module. If it does, make sure that it is removed. Guard particularly against wire offcuts.

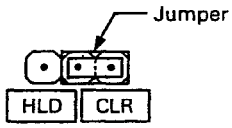
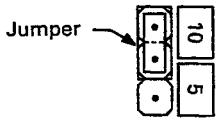
(4) Tighten the screws as specified below:

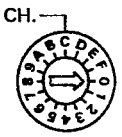
Screw	Tightening Torque Range
I/O terminal screw (M3 screw)	39 to 59 N·cm
I/O terminal block installation screw (M4 screw)	78 to 118 N·cm

(5) To load the module onto the base, press the module against the base so that the catch on the top of the unit is securely locked. To unload the module, push the catch, and after the catch is disengaged from the base, pull the module toward you.

4.3 Nomenclature



No.	Description	Application
①	Analog output HOLD/CLEAR setting pins 	1) Used to hold or clear analog output at the time of ACPU stop. 2) Factory-set to "CLR".
②	Output voltage range setting pins 	1) Used to specify the range of voltage output from the A616DA. 2) Allows "10V" or "5V" to be specified per channel. 3) Factory-set to "10V".
③	Test mode terminals	Used to select normal or test mode. (a) Disconnected ··· Normal mode (to output analog values to external devices) (b) Connected ····· Test mode (to set offset/gain values)
④	Power terminals	1) Input terminals for analog value output power supply (±15V DC). 2) Used for analog value output.

No.	Description	Application
⑤	"RUN" LED	1) Indicates the operating status of the A616DA. 2) Normal mode (a) On ····· Indicates that the A616DA is operating without fault. (b) Off ····· • 5V DC is not supplied to the A616DA. • A616DA is in WDT error. • A616DA hardware fault has occurred. • ACPU has detected an error and stopped operation. (c) Fast flicker ····· (at intervals of 0.1sec) • Offset/gain value setting is not normal. • A616DA hardware fault. 3) Test mode (a) Flicker { At intervals of 0.5sec ···· • OFFSET/GAIN select switch is in "OFFSET" or "GAIN" position. At intervals of 0.1sec ···· • The high or low limit of the allowed range has been exceeded during offset/gain value setting using the UP/DOWN switch. • Offset value setting is greater than gain value setting using the UP/DOWN switch. (b) Off ····· OFFSET/GAIN select switch is in "SET" position.
⑥	Channel select switch 	1) Used to specify the channel (CH.0 to F) for offset/gain adjustment. 2) Channel should be switched when the OFFSET/GAIN select switch is in "SET" position. 3) Only valid in test mode.
⑦	OFFSET/GAIN select switch	Used to select any of the following modes: (a) OFFSET position ····· Offset value calibration mode. (b) GAIN position ····· Gain value calibration mode. (c) SET position ····· Offset/gain value storage mode. (The offset/gain value is stored to the A616DA internal memory when the switch is moved from "OFFSET"/"GAIN" to "SET".)
⑧	UP/DOWN switch	1) Used to define the offset/gain value for the specified channel. 2) Increases or decreases the offset or gain value at the following rate: (a) UP/DOWN position for less than 1.5 seconds: Increase or decrease of 0.65mV (1.3mV) at one time.* (b) UP/DOWN position for 1.5 seconds or more: Increase or decrease of 0.65mV (1.3mV) per 0.05sec.

REMARKS

1)* ····· A change of 1.3mV for the output voltage range of −10V to 0V to +10V and 0.65mV for −5V to 0V to +5V.

4.4 Settings

The following settings should have been performed before loading the A616DA to the base unit.

4.4.1 Setting analog output to HOLD/CLEAR

Set analog output at ACPU STOP to HOLD or CLEAR by inserting the jumper into the pins on the left-hand side of the A616DA.

(a) Setting analog output to HOLD:
Set the HOLD/CLEAR setting jumper to the "HLD" position. (See Fig. 4.2.)
(b) Setting analog output to CLEAR:
Set the HOLD/CLEAR setting jumper to the "CLR" position. (See Fig. 4.2.)

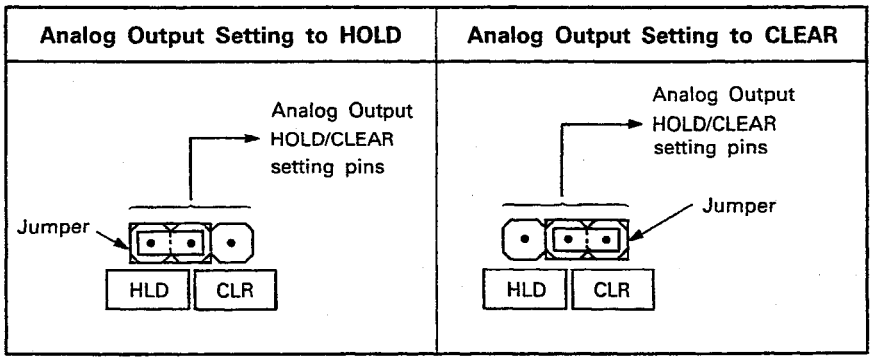


Fig. 4.2 Analog Output HOLD/CLEAR Setting

4.4.2 Setting the output voltage range

Define the output voltage range ("−10V to 0V to +10V" or "−5V to 0V to +5V") by inserting the jumper into the pins on the left-hand side of the A616DA.

(a) Setting to "−10V to 0V to +10V":
Set the output voltage range setting jumper to the "10" position. (See Fig. 4.3.)

(b) Setting to "−5V to 0V to +5V":
Set the output voltage range setting jumper to the "5" position. (See Fig. 4.3.)

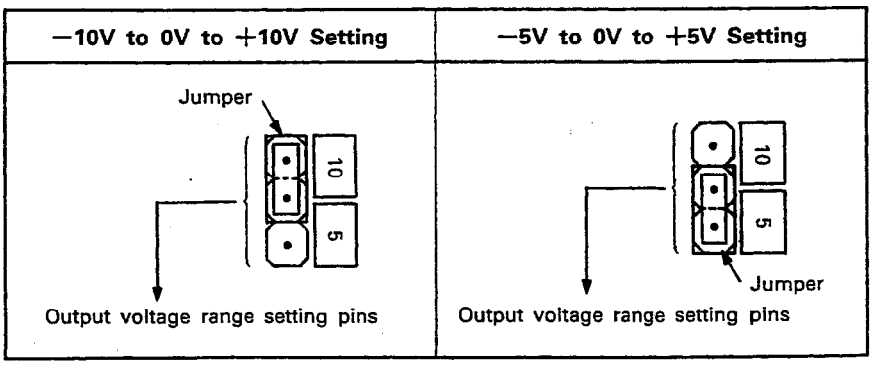


Fig. 4.3 Output Voltage Range Setting

4.5 Offset/Gain Setting

(1) The offset and gain values are factory-set to output the voltages indicated in Table 4.1.

Output Voltage Range Setting	10V setting
Gain value (V)	10
Offset value (V)	0

Table 4.1 Factory-Set Offset/Gain Values

(2) The offset and gain values may be changed and fine-adjusted by offset/gain setting in test mode.

4.5.1 Notes on offset/gain setting

(1) Do not select test mode during execution of D/A conversion. Selecting test mode stops D/A conversion of all channels and affects control of external devices. Returning from test mode to normal mode resumes D/A conversion with new offset/gain values.

(2) Offset/gain setting is allowed within the following ranges:
(a) Output voltage range is 10V ····· −10V to 0V to +10V
(b) Output voltage range is 5V ····· −5V to 0V to +5V
If any value set is outside the above range, overall accuracy may not be within the range of performance specifications (see Section 3.2.).

(3) The defined value is stored when the OFFSET/GAIN select switch is set to the "SET" position.
The offset and gain value remain unchanged if test mode is terminated with the OFFSET/GAIN select switch in the "OFFSET" or "GAIN" position.

(4) Before switching from one channel to another in test mode, the OFFSET/GAIN select switch should be set to the "SET" position.
If the channel is switched with the OFFSET/GAIN select switch in the "OFFSET" or "GAIN" position, the offset/gain value of the previous channel remains unchanged and the set value is stored to the new channel when the switch is set to "SET".

Example

(1) The gain value of channel 3 has been changed from 10V to 5V and channel 4 has been selected with the OFFSET/GAIN select switch in the "GAIN" position.
(a) Gain value of channel 3 ····· Remains 10V.
(b) Gain value of channel 4 ····· 5V is output.
5V is stored as a gain value when the OFFSET/GAIN select switch is set to "SET".

(5) The "RUN" LED flickers fast at intervals of 0.1 seconds to indicate that the offset/gain value specified has exceeded the allowed range.
When the "RUN" LED is flickering fast, the offset/gain value remains unchanged if the OFFSET/GAIN select switch is set to "SET".

4.5.2 Offset/gain setting procedure

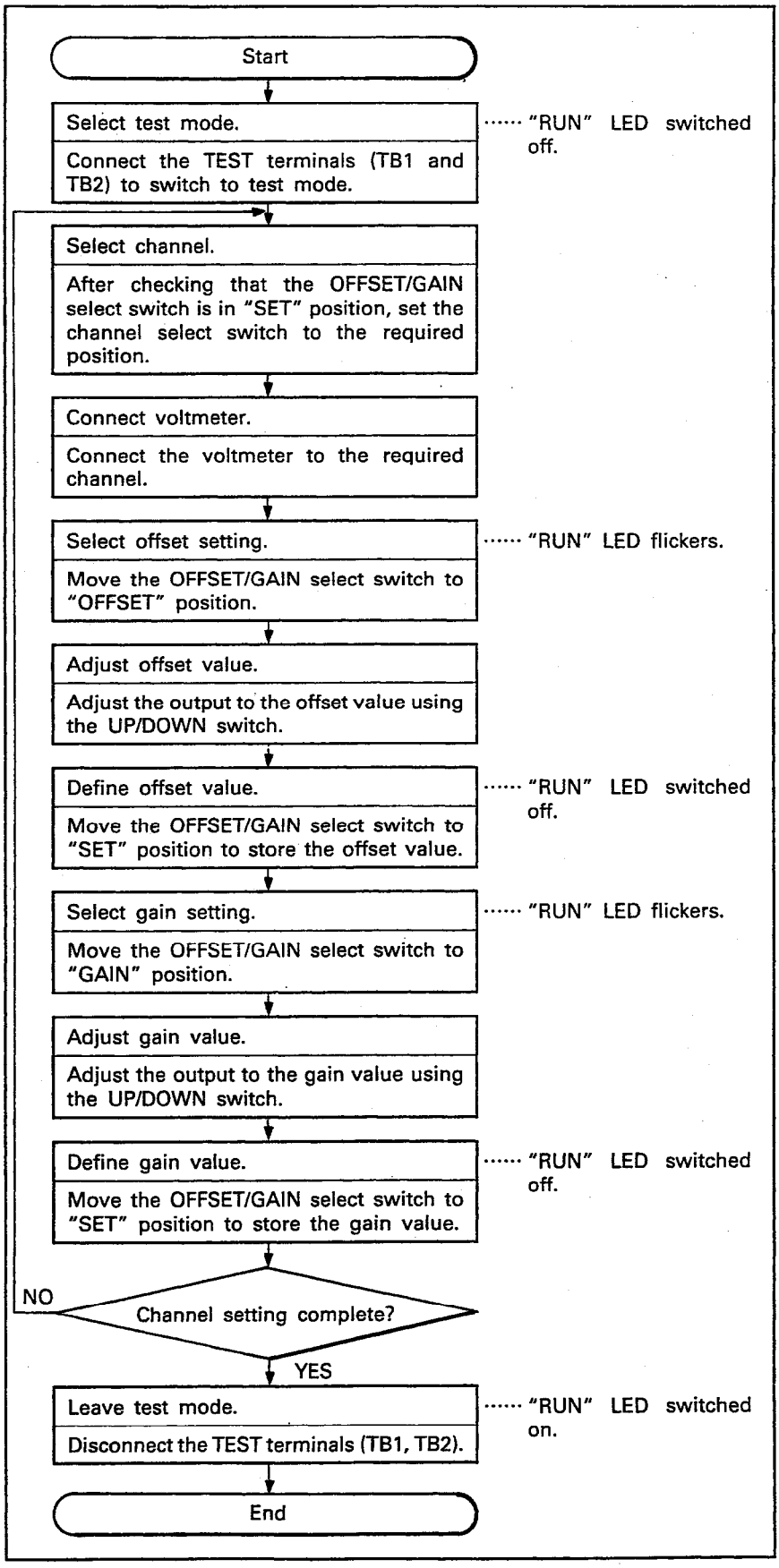


Fig. 4.4 Offset/Gain Setting Procedure

4.6 Wiring

4.6.1 Wiring instructions

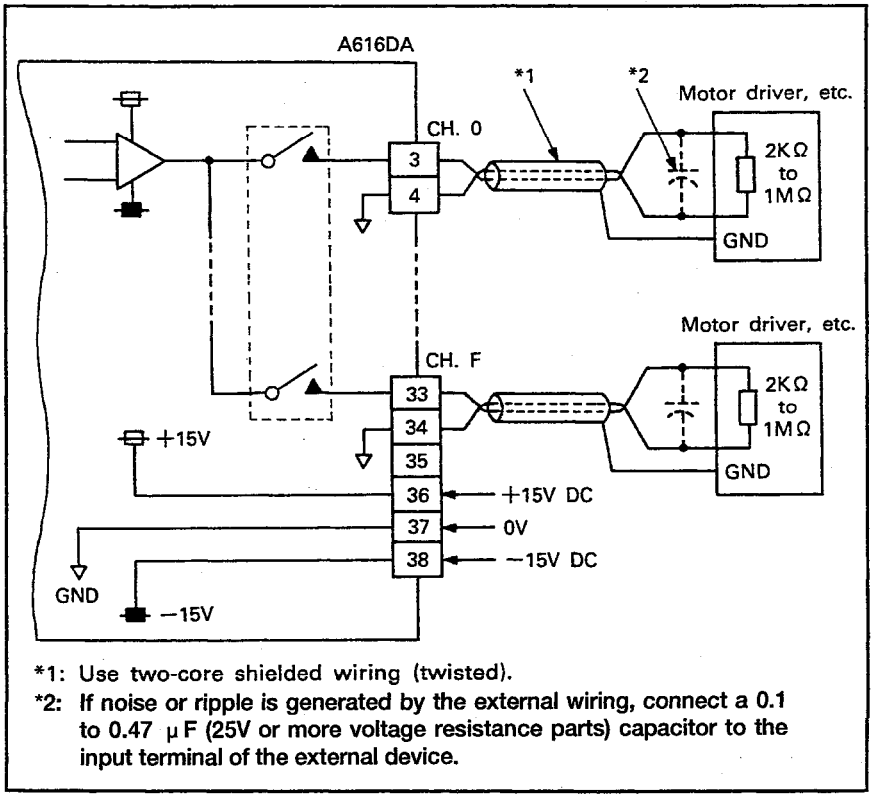
Protect external wiring against noise with the following precautions:

(1) Separate AC and DC wiring.

(2) Separate main circuit and/or high voltage wiring from control and signal wiring.

(3) Where applicable, ground the shielding of all wires to a common ground point.

4.6.2 Connection of A616DA and external devices



*1: Use two-core shielded wiring (twisted).
*2: If noise or ripple is generated by the external wiring, connect a 0.1 to 0.47 μF (25V or more voltage resistance parts) capacitor to the input terminal of the external device.

Fig. 4.5 Connection Example of A616DA and External Devices

4.6.3 Connection of ±15V DC to the A616DA

±15V DC may be supplied to the A616DA in either of the following ways:

(a) A68P power supply module

(b) External power supply

Use of the A68P power supply module

(1) Connect the +15V, 0V and −15V terminals of the A616DA with those of the A68P.

(2) One A68P can supply ±15V DC to four A616DAs.

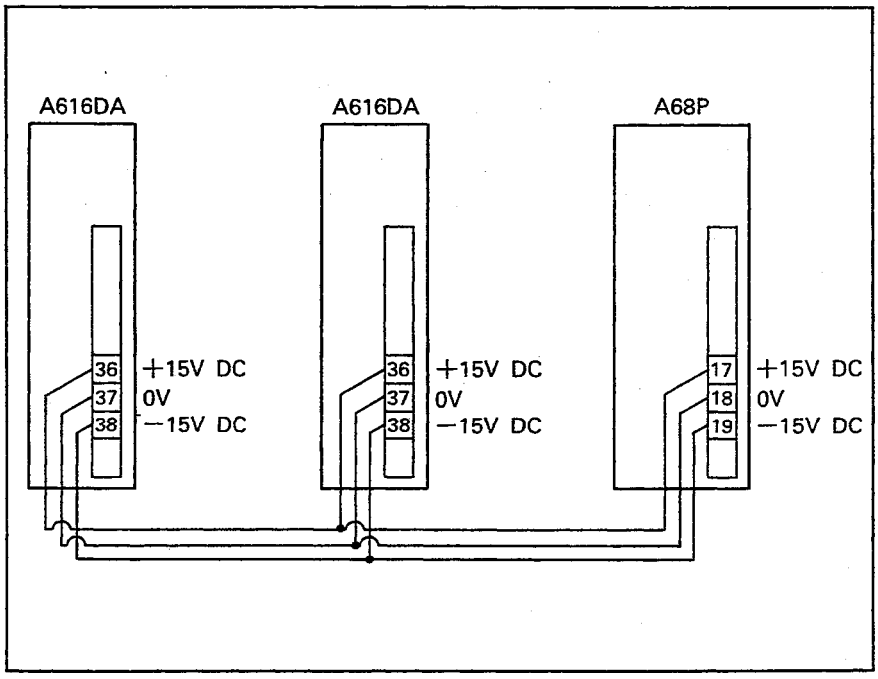


Fig. 4.6 Connection of ±15V DC to the A616DA (using the A68P)

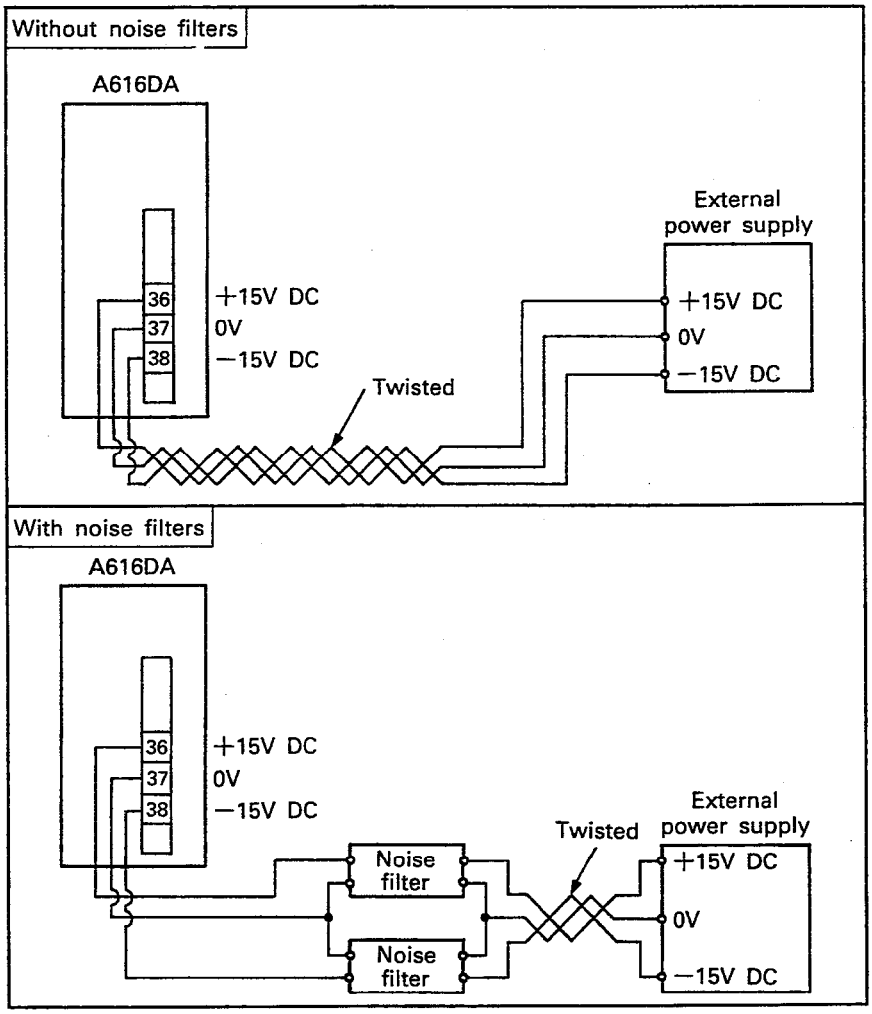
(3) To protect the A616DA, ±15V DC must not be supplied to one A616DA from several A68Ps connected in parallel.

Use of external power supply

(1) Connect the +15V, 0V and −15V terminals of the A616DA with those of the external power supply.

(2) When the external power supply is used, it is recommended to use noise filters with the A616DA:

(3) The power specifications of the external power supply is given in Section 3.7.



POINT

(1) The cables between the noise filters and A616DA must not be bundled with any other cable.

(2) The cables between the noise filters and A616DA must be as short as possible.

MEMO

5. PROGRAMMING

This section explains the programming procedure for use of the A616DA. When applying any of the program examples introduced in this chapter to the actual system, verify the applicability and confirm that no problems will occur in the system control.

5.1 Programming Procedure

Program data transfer between the ACPU and A616DA as indicated in Fig. 5.1.

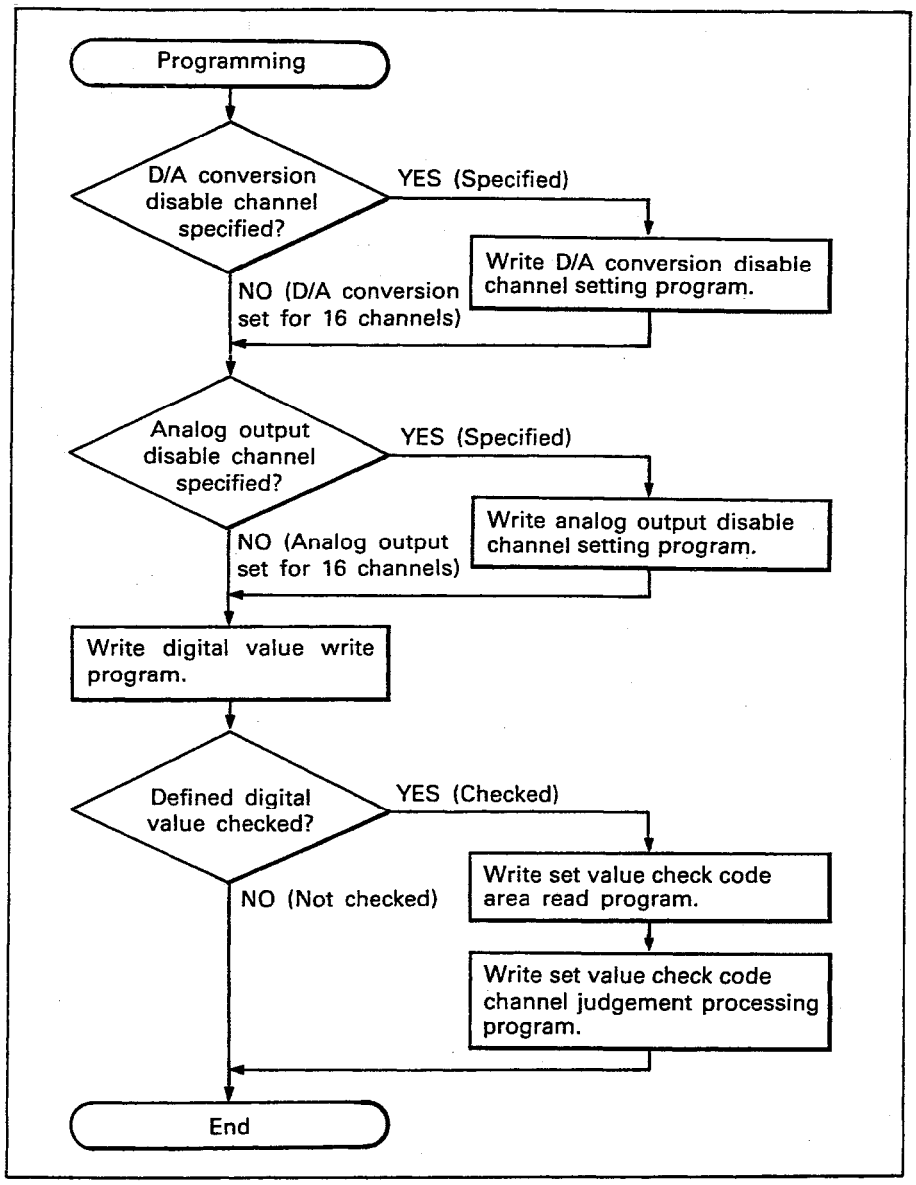


Fig. 5.1 Programming Procedure

POINT

During each of the processes of the special function module, access from the PLC CPU will have priority. Accordingly, if frequent access to the buffer memory of the special function module made from the PLC CPU, it will not only extend the scan time of the PLC CPU, delays in each of the processes of the special function module will occur. Only use the FROM/TO and other such commands to access the buffer memory from the PLC CPU when necessary.

5.2 I/O List for ACPU

5.2.1 Input list

(1) Input signals given from the A616DA to the ACPU are X_n0 to $X_{(n+1)}F$* (32 points).

(2) Input signal specifications

Input Signal	Name	Description
X_n0	Watch dog timer error	Switched on if a watch dog timer error occurs in the A616DA.
X_n1	D/A conversion ready flag	Normal mode (other than test mode) (1) Switched on when D/A conversion is ready after the ACPU is powered up or reset. (2) Switched off if: (a) WDT error occurs in the A616DA (b) A616DA hardware fault occurs; or (c) ACPU has detected an error and stopped operation. (3) Data transfer between ACPU and A616DA is made after X_n1 is switched on. (X_n1 is used as a read/write interlock.) Test mode Switched off when normal mode is switched to test mode.
X_n2	Error flag	(1) Switched on if the digital input from the ACPU for any channel is outside the allowed range (—4096 to 4095). (2) Switched off when all values in the buffer memory error code area (30_H to $3F_H$) are set to 0.
X_n3 to $X_{(n+1)}C$	——	Reserved.
$X_{(n+1)}D$ to $X_{(n+1)}F$	RFRP, RTOP instruction interlock signals	Only used when the A616DA is loaded into a remote I/O station.

Table 5.1 Input Signal Specifications

REMARKS

1) * ····· n in X_n0 to $X_{n+1}F$ indicates the head address of the slot being used for the A616DA.

Example

n = 00 if the A616DA is used on slot 0 of the main base.

X_n0 → X000

n

5.2.2 Output list

(1) Output signals given from the ACPU to the A616DA are Y_n0 to $Y_{(n+1)}F$* (32 points).

(2) Output signal specifications

Output Signal	Name	Description
Y_n0 to Y_nC	——	Reserved.
Y_nD to Y_nF	RFRP, RTOP instruction interlock signals	Only used when the A616DA is loaded into a remote I/O station.
$Y_{(n+1)}0$ to $Y_{(n+1)}A$	——	Reserved.
$Y_{(n+1)}B$	Output batch enable flag	(1) Shared among channels 0 to F. (2) For analog output in normal mode, see Table 3.4. (3) In test mode, offset/gain values are output independently of the ON/OFF state of the output batch enable flag.
$Y_{(n+1)}C$ to $Y_{(n+1)}F$	——	Reserved.

Table 5.2 Output Signal Specifications

IMPORTANT

Y_n0 to Y_nC, $Y_{(n+1)}0$ to $Y_{(n+1)}A$, and $Y_{(n+1)}C$ to $Y_{(n+1)}F$ are reserved for the system and must not be used (switched on/off) in the sequence program.

REMARKS

1) * ····· n in Y_n0 to $Y_{n+1}F$ indicates the head address of the slot being used for the A616DA.

Example

n = 00 if the A616DA is used on slot 0 of the main base.

Y_n0 → X000

n

5.3 Buffer Memory

(1) The A616DA has a buffer memory (not battery backed) for data communication with the ACPU.

(2) The buffer memory assignment and data maps are indicated below.

5.3.1 Buffer memory assignment

Address (Hexadecimal)		Communication with ACPU		Relevant Section
		Read	Write	
0	D/A conversion enable/disable channel	○	○	Section 5.3.2
1	Analog output enable/disable channel	○	○	Section 5.3.3
2 to F	Reserved	–	–	–
10	CH. 0 digital value	○	○	Section 5.3.4
11	CH. 1 digital value			
12	CH. 2 digital value			
13	CH. 3 digital value			
14	CH. 4 digital value			
15	CH. 5 digital value			
16	CH. 6 digital value			
17	CH. 7 digital value			
18	CH. 8 digital value			
19	CH. 9 digital value			
1A	CH. A digital value			
1B	CH. B digital value			
1C	CH. C digital value			
1D	CH. D digital value			
1E	CH. E digital value			
1F	CH. F digital value			
20 to 2F	Reserved	–	–	–
30	CH. 0 set value check code	○	○	Section 5.3.5
31	CH. 1 set value check code			
32	CH. 2 set value check code			
33	CH. 3 set value check code			
34	CH. 4 set value check code			
35	CH. 5 set value check code			
36	CH. 6 set value check code			
37	CH. 7 set value check code			
38	CH. 8 set value check code			
39	CH. 9 set value check code			
3A	CH. A set value check code			
3B	CH. B set value check code			
3C	CH. C set value check code			
3D	CH. D set value check code			
3E	CH. E set value check code			
3F	CH. F set value check code			

*○····· Accessible

Fig. 5.2 Buffer Memory Assignment

5.3.2 D/A conversion enable/disable channel area (Address 0_H)

(1) Defines whether D/A conversion is performed or not on a channel-by-channel basis.

(2) All channels are enabled for D/A conversion when:
  (a) Power is switched on; or
  (b) ACPU is reset.

(3) D/A conversion enable/disable is defined by 1/0.
  (a) Enable·····1
  (b) Disable·····0

(4) The D/A conversion enable/disable channel area data map is shown below:

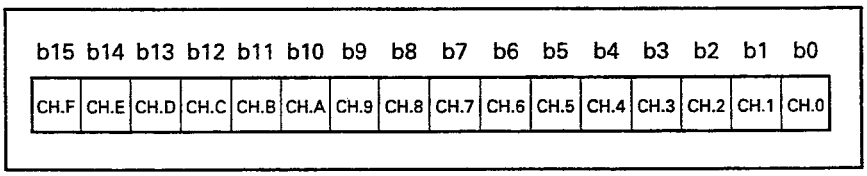


Fig. 5.3 D/A Conversion Enable/Disable Channel Area Data Map

5.3.3 Analog output enable/disable channel area (Address 1_H)

(1) Defines output enable/disable for the converted analog value per channel.

(2) All channels are enabled for output when:
  (a) Power is switched on; or
  (b) ACPU is reset.

(3) Output enable/disable is defined by 1/0.
  (a) Enable·····1
  (b) Disable·····0

(4) The analog output enable/disable channel area data map is shown below:

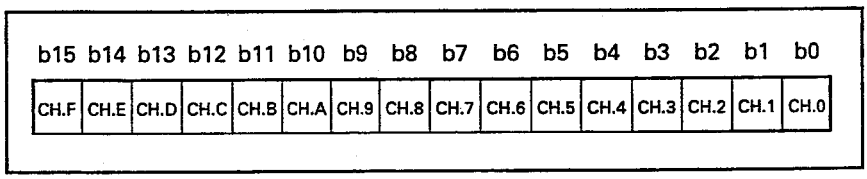


Fig. 5.4 Analog Output Enable/Disable Channel Area Data Map

5.3.4 CH.0 to CH.F digital value area (Addresses 10_H to $1F_H$)

(1) Write digital values to this area from the ACPU for D/A conversion.

(2) Digital values of all channels are set to 0 if:
(a) D/A conversion ready (X01) is on after power on; or
(b) D/A conversion ready (X01) is switched on after the ACPU is reset.

(3) Any digital value specified should be a 16-bit signed binary between −4096 and +4095. Any digital value outside this range is changed to a value indicated below before D/A conversion, and the corresponding check code is written to the set value check code area (addresses 30_H to $3F_H$).
(a) −4097 to −32768 ⟶ −4096
(b) 4096 to 32767 ⟶ 4095

5.3.5 CH.0 to CH.F set value check code area (Addresses 30_H to $3F_H$)

(1) Checks whether the set digital values are within or outside the range −4096 to 4095.

(2) The corresponding code in Table 5.3 is written if a digital value outside the above range is specified.

Check Code	Description
$000F_H$	Digital value specified is 4096 or greater.
$00F0_H$	Digital value specified is −4097 or less.
$00FF_H$	Digital values specified are outside the range −4096 and 4095. For example, after writing a digital value of 4096 or greater, writing another value of −4097 or less without resetting the check code will store check code $00FF_H$.

Table 5.3 Check Code List

(3) Any check code written is not reset if the corresponding set value is corrected to a valid value (within the range −4096 to 4095).
The check code should be reset by the sequence program.

POINT

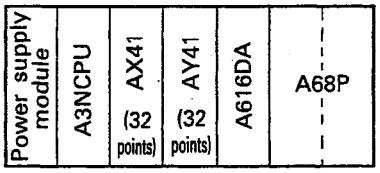
The error flag (X_n2) is switched on to indicate that a check code has been written to the set value check code area.

5.4 Program Examples for Building Block Type CPU

5.4.1 Digital value setting program

The following program writes a value (0 to 4000) defined by the BCD digital switch to channels 0 to 3 of the A616DA.
(This program includes a program for disabling channels 4 to F for D/A conversion and analog output.)

【Module arrangement】



X00	Y20	X/Y40	60	70
to	to	to	to	to
X1F	Y3F	X/Y5F	6F	7F

} ····· I/O numbers

【Specifications】

(1) Executed commands

(a) D/A conversion disable channel setting command ····· X0

(b) Analog output disable channel setting command ····· X1

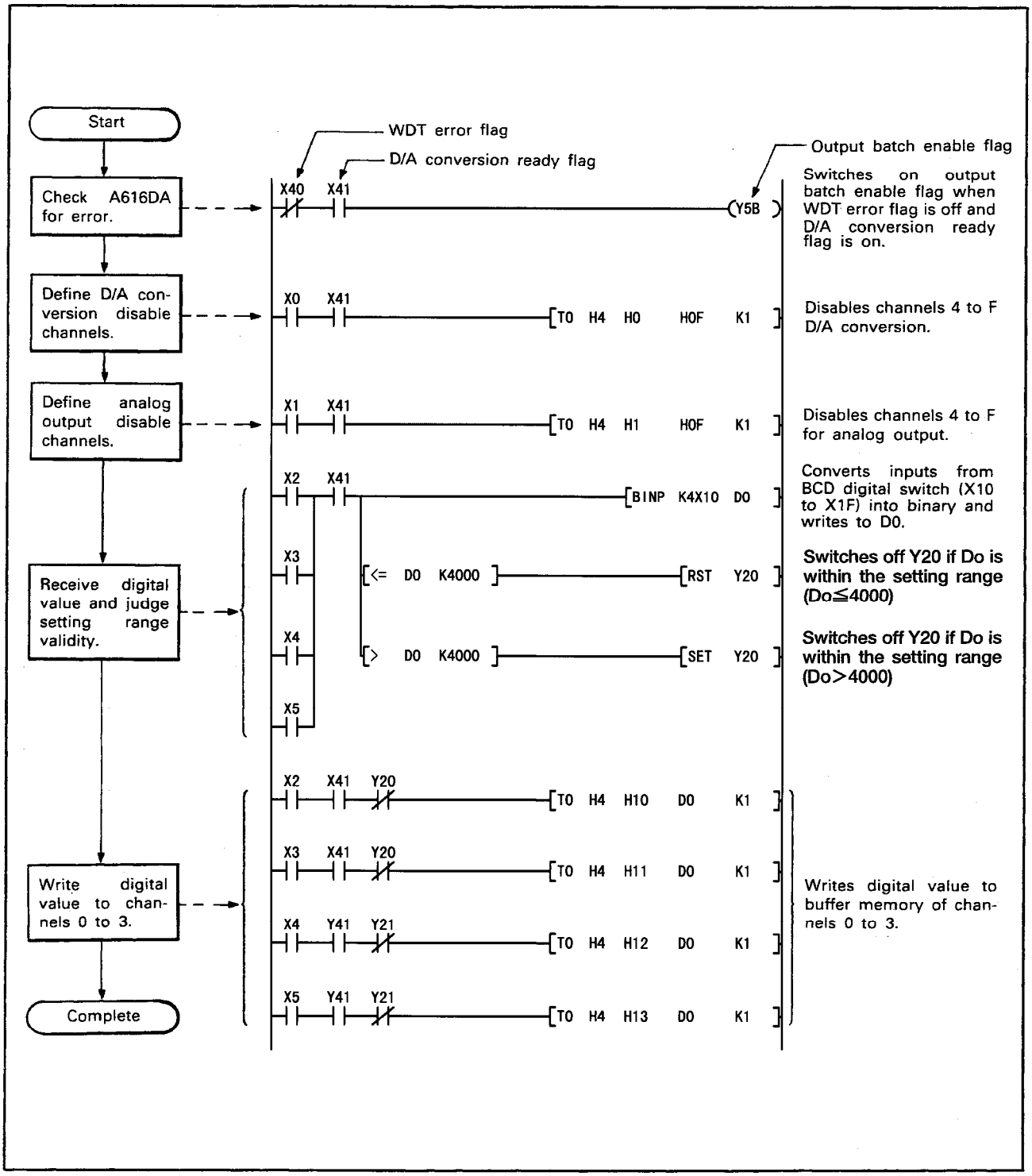
(c) Digital value setting commands
1) Channel 0 ····· X2
2) Channel 1 ····· X3
3) Channel 2 ····· X4
4) Channel 3 ····· X5

(2) Digital value setting (4 BCD digits) ····· X10 to X1F

(3) Digital value setting error output ····· Y20

(4) Register for storing digital value ····· D0

【Program example】



POINT

It is also acceptable to use the TOP command in the locations using the TO command in the program example shown above.

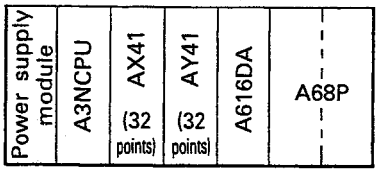
5.4.2 Digital value setting error detection program

The following program detects any digital value outside the range —4096 to 4095 and outputs the corresponding channel to Y30-Y37 in BCD.

Example

1) Channel "0" ····· 1 output to Y30-Y37.
2) Channel "F" ····· 16 output to Y30-Y37.

【Module arrangement】



X00	Y20	X/Y40	60	70
to	to	to	to	to
X1F	Y3F	X/Y5F	6F	7F

} ····· I/O numbers

【Specifications】

(1) Executed commands

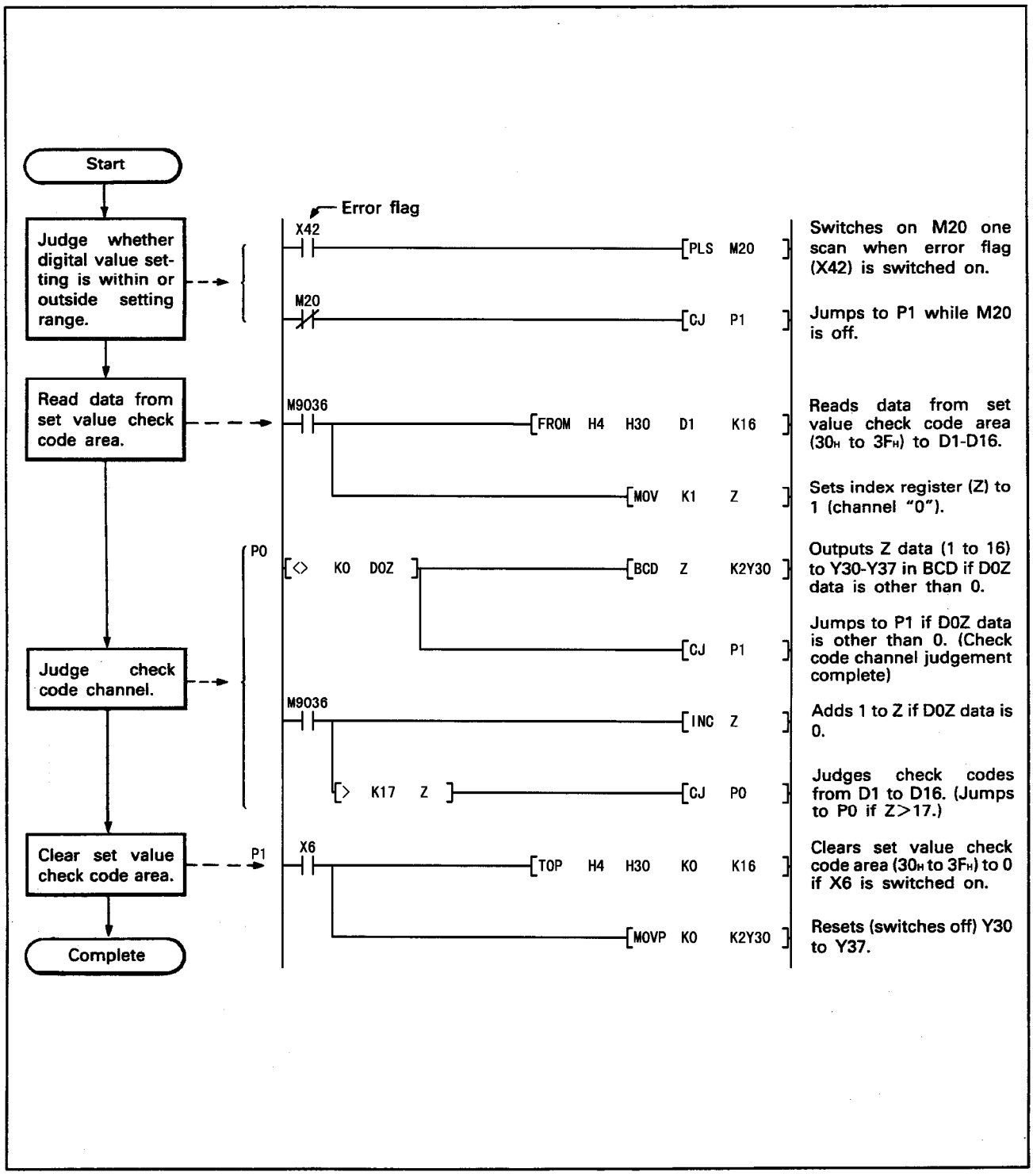
(a) Judgement of digital value defined outside the setting range····· X42 (error flag)

(b) Error flag off command ····· X6

(c) Check code register judgement command····· M20

(2) Registers for storing set value check code area data D1 to D16

[Program example]



POINT

In the above program, only the lowest faulty channel number is displayed if two or more channels result in setting error at the same time.

5.4.3 Program for the A616DA loaded in remote I/O station

The following program is used to write a value (0 to 4000) defined by the BCD digital switch to channels 0 to 3 of the A616DA in a remote I/O station.
(This program includes a program for disabling channels 4 to F for D/A conversion and analog output.)

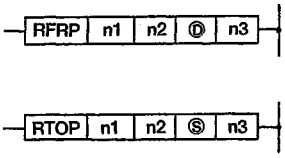
【Instructions】

(1) Data transfer method
The ACPU has direct and refresh I/O control modes. Data transfer between the ACPU and remote I/O station is made in batch refresh mode after execution of the END (FEND) instruction.

(2) Response delay
A time difference (response delay) occurs because control data transferred between the master station CPU and remote I/O station A616DA is controlled through the link module. Control timing must therefore be noted.

(3) Instructions used
The following instructions are used for data transfer between the master station CPU and remote I/O station A616DA:

(a) Data write (master station to A616DA) ····· RTOP instruction
(b) Data read (A616DA to master station) ····· RFRP instruction



Setting data

n1		First I/O number (3 digits) of the special function module specified by the master station.
n2	RFRP	Address inside the special function module that is storing the read data.
	RTOP	Address inside the special function module that reads the data.
Ⓓ	RFRP	First number of the link register that stores the data that has been read.
Ⓢ	RTOP	First number of the link register that the write data is storing.
n3		Read, write data number (1 to 16)

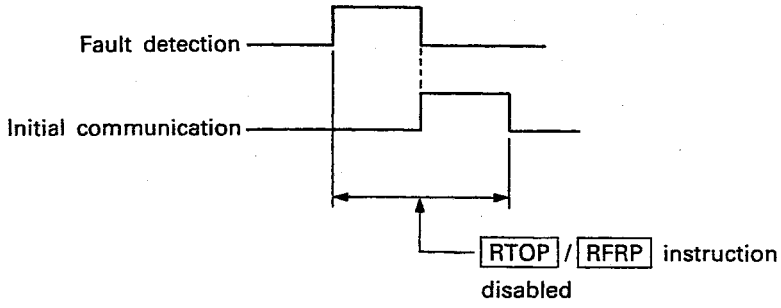
(4) Device for data transfer
Link registers (W) are used for data transfer between the master station CPU and remote I/O station A616DA. Write either or both of the following programs to the master station as appropriate:

(a) Data write ····· Program which transfers data (to be transferred to the remote I/O station A616DA) to the specified link registers before execution of the RTOP instruction.
(b) Data read ····· Program which transfers data from the link registers to the other device after execution of the RFRP instruction.

(5) Disabled simultaneous execution of [RTOP] and [RFRP] instructions
The [RTOP] and [RFRP] instructions cannot be executed at the same time to one A616DA. To enable simultaneous execution, data link I/O signals must be written in the program as interlock conditions.
(When two A616DAs are loaded in the remote I/O station, the [RTOP] instruction may be executed to one A616DA and the [RFRP] instruction to the other at the same time.)

(6) Control signals to the A616DA
Because of the relation between the master station scan time and link scan time, the PLS Y[ ] signal output to the remote I/O station may not be provided to the A616DA.
The pulse output which executes the [RST] instruction after the [SET] instruction cannot be used because data is transferred between the master station and remote I/O station in batch refresh mode after execution of the [END] (FEND) instruction.

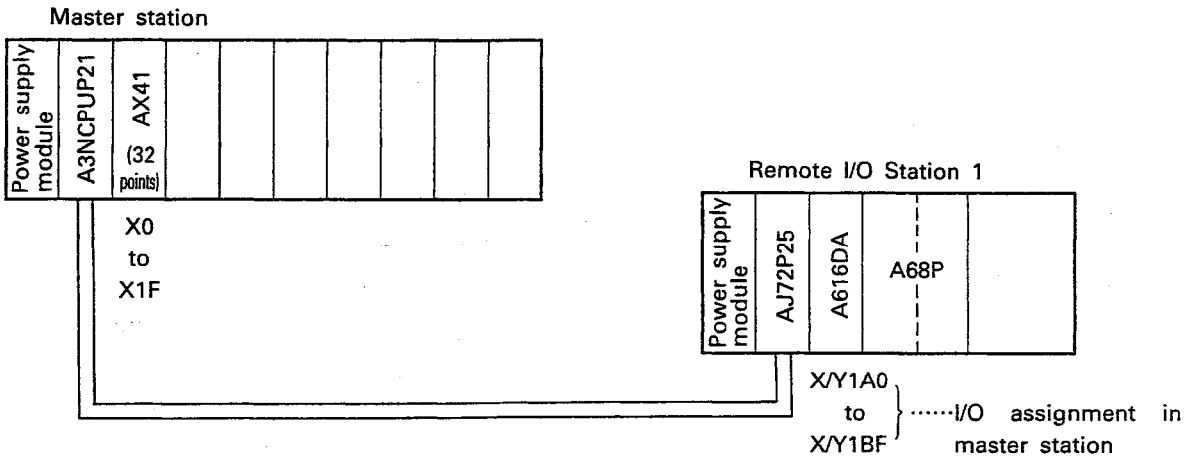
(7) Detection of remote I/O station fault or parameter communication
(a) Provide interlock using the following devices so that the [RTOP]/[RFRP] instruction is not executed when the remote I/O station is faulty or during initial communication with the remote I/O station.
1) Remote I/O station fault detection ····· D9228 to D9231
2) Initial communication detection ····· D9224 to D9227
The remote I/O station fault and initial communication detection timings are as shown below:



(b) The fault detection program must be written before the initial communication detection program.
If these programs are written in reverse order, neither fault nor initial communication may be detected depending on the link refresh timing.

(8) A616DA fault detection
(a) $X_{(n+1)}D$ is switched on to indicate that the A616DA is faulty and the [RFRP]/[RTOP] instruction cannot be executed. In this case, check the A616DA for A616DA fault, module loading fault, etc.
(b) Switch on Y_nD to switch off $X_{(n+1)}D$.
Y_nD must only be switched on/off as described below by using the [SET]/[RST] instruction:
1) Switched on when $X_{(n+1)}D$ is switched on.
2) Switched off only once when $X_{(n+1)}D$ is switched off.

【Module Assignment】



【Specifications】

(1) Executed commands
- (a) D/A conversion disable channel setting command ····· X0
- (b) Analog output disable channel setting command ····· X1
- (c) Digital value setting commands
  - 1) Channel 0 ····· X2
  - 2) Channel 1 ····· X3
  - 3) Channel 2 ····· X4
  - 4) Channel 3 ····· X5

(2) Digital value setting (4 digit BCD) ····· X10 to X1F

(3) Registers for storing digital value
- 1) D/A conversion disable channel ····· W305
- 2) Analog output disable channel ····· W306
- 3) Channel 0 ····· W307
- 4) Channel 1 ····· W308
- 5) Channel 2 ····· W309
- 6) Channel 3 ····· W30A

Point

(1) The link register shown in the specifications above indicates when W304 to W30A are set by the link parameters for writing from the master station to the No.1 PLC of remote I/O station.

Link setting

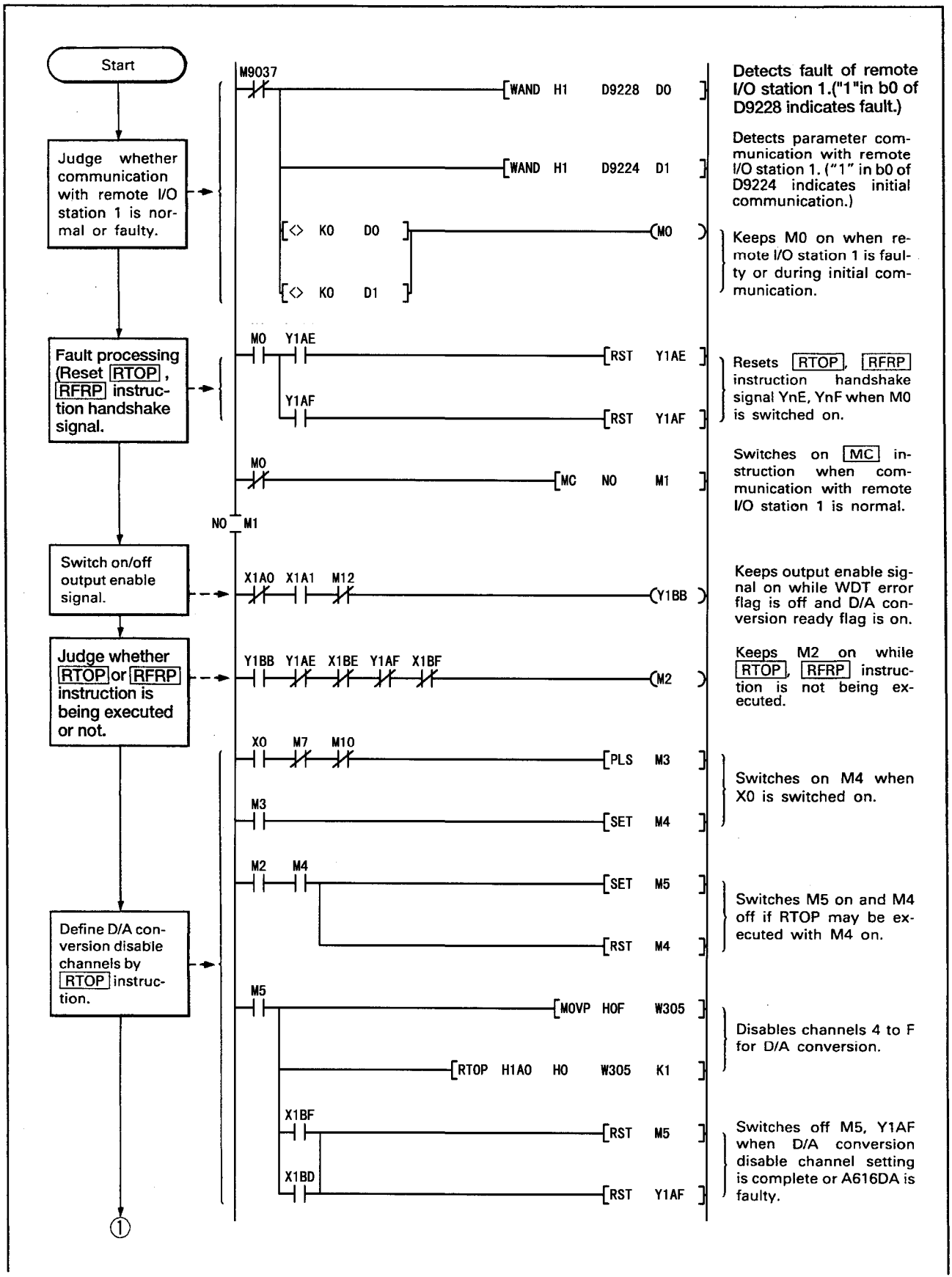
Master	Slave PC STN.	M→ All L		Link WDT 10ms
		B	W	
M	1	—	—	200

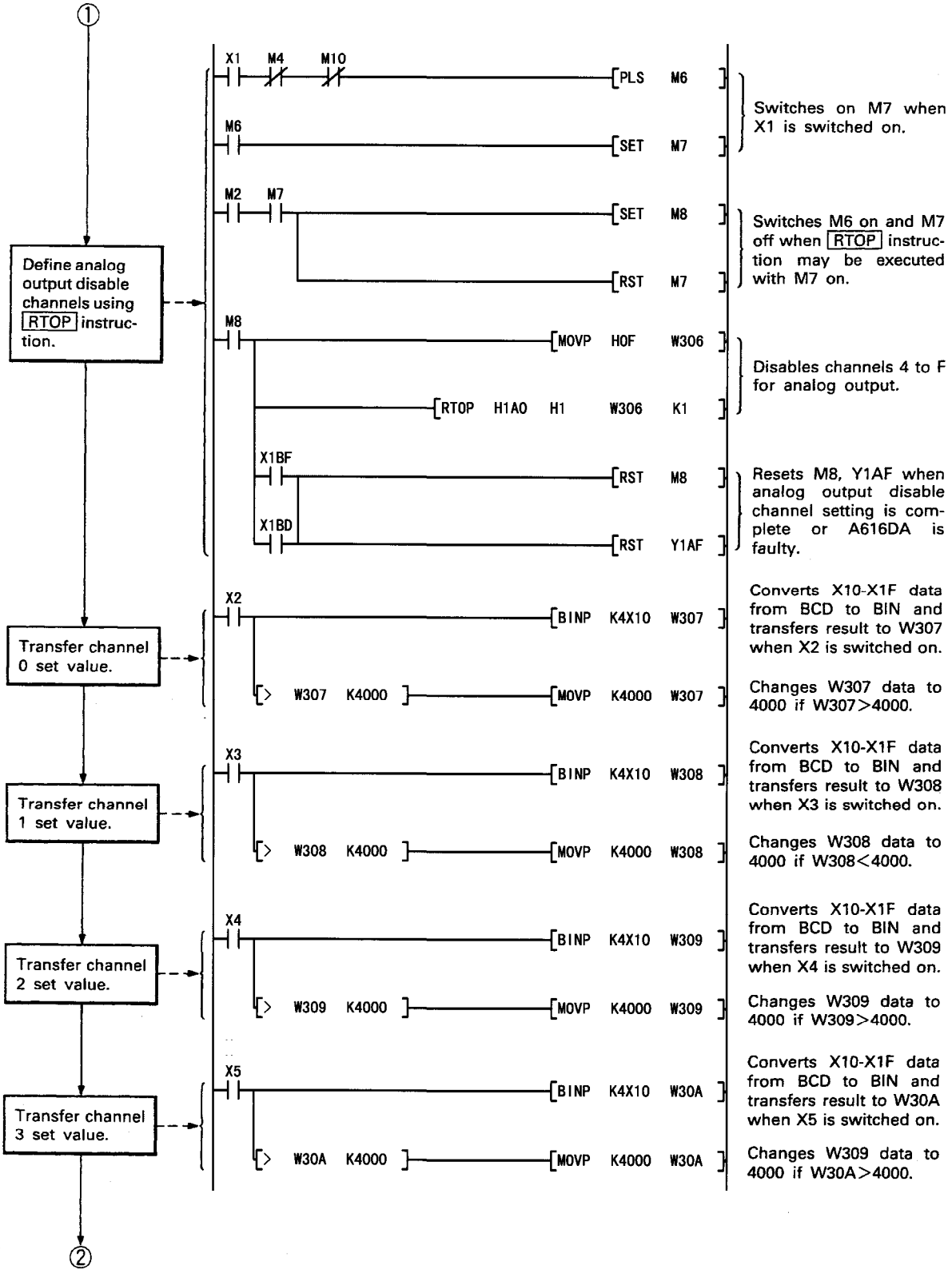
M : B ⟶ ALL L : B -
M : W ⟶ ALL L : W -
M : W ⟶ ALL R : W 304-30A
M : W ⟶ ALL R : W -
M : Y ⟶ ALL L : X -
M : Y ⟶ ALL R : Y 1A0-1BF
M : X ⟶ ALL L : Y -
M : X ⟶ ALL R : X 1A0-1BF

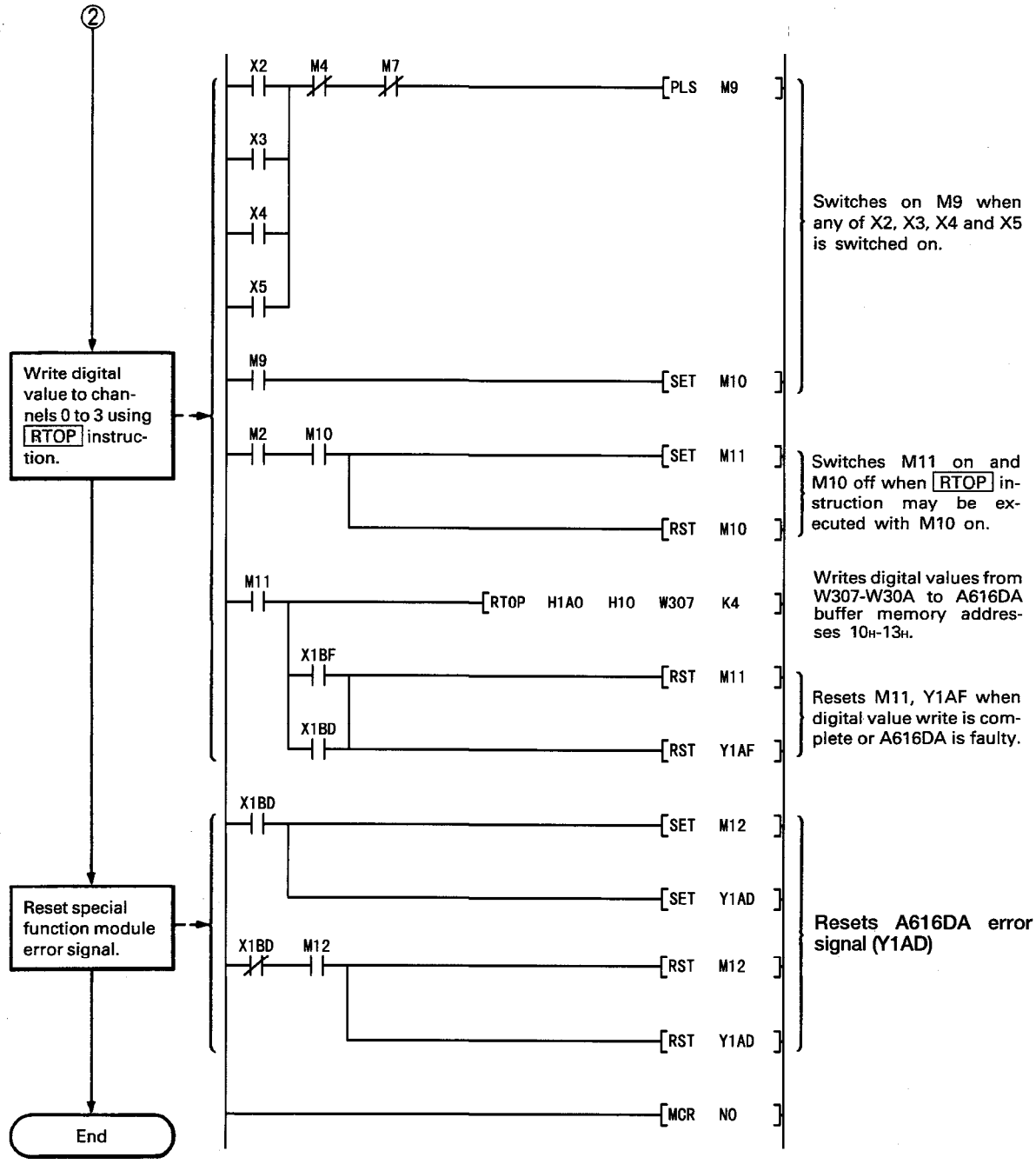
L/R NO.	M ← L		M → R	M ← R	M → L/R		M ← L/R	
	B	W	W	W	Y	X/Y	X	Y/X
R 1	-------- -	-------- -	304-30A -	-	1A0-1BF	000-01F	1A0-1BF	000-01F

With the W304, since the OS is used for address storage for A616DA of the No.1 PLC of the remote I/O station, data cannot be stored by the user.

【Program example】




①
Define analog output disable channels using RTOP instruction.
X1 M4 M10 PLS M6
M6 SET M7
Switches on M7 when X1 is switched on.
M2 M7 SET M8
RST M7
Switches M6 on and M7 off when RTOP instruction may be executed with M7 on.
M8 MOVP H0F W306
RTOP H1A0 H1 W306 K1
Disables channels 4 to F for analog output.
X1BF RST M8
X1BD RST Y1AF
Resets M8, Y1AF when analog output disable channel setting is complete or A616DA is faulty.
Transfer channel 0 set value.
X2 BINP K4X10 W307
Converts X10-X1F data from BCD to BIN and transfers result to W307 when X2 is switched on.
> W307 K4000 MOVP K4000 W307
Changes W307 data to 4000 if W307>4000.
Transfer channel 1 set value.
X3 BINP K4X10 W308
Converts X10-X1F data from BCD to BIN and transfers result to W308 when X3 is switched on.
> W308 K4000 MOVP K4000 W308
Changes W308 data to 4000 if W308<4000.
Transfer channel 2 set value.
X4 BINP K4X10 W309
Converts X10-X1F data from BCD to BIN and transfers result to W309 when X4 is switched on.
> W309 K4000 MOVP K4000 W309
Changes W309 data to 4000 if W309>4000.
Transfer channel 3 set value.
X5 BINP K4X10 W30A
Converts X10-X1F data from BCD to BIN and transfers result to W30A when X5 is switched on.
> W30A K4000 MOVP K4000 W30A
Changes W309 data to 4000 if W30A>4000.
②


②
X2
M4
M7
PLS M9
X3
X4
X5
Switches on M9 when any of X2, X3, X4 and X5 is switched on.
Write digital value to channels 0 to 3 using RTOP instruction.
M9
SET M10
M2
M10
SET M11
RST M10
Switches M11 on and M10 off when RTOP instruction may be executed with M10 on.
M11
RTOP H1A0 H10 W307 K4
Writes digital values from W307-W30A to A616DA buffer memory addresses 10H-13H.
X1BF
RST M11
X1BD
RST Y1AF
Resets M11, Y1AF when digital value write is complete or A616DA is faulty.
X1BD
SET M12
SET Y1AD
Reset special function module error signal.
X1BD
M12
RST M12
RST Y1AD
Resets A616DA error signal (Y1AD)
MCR N0
End

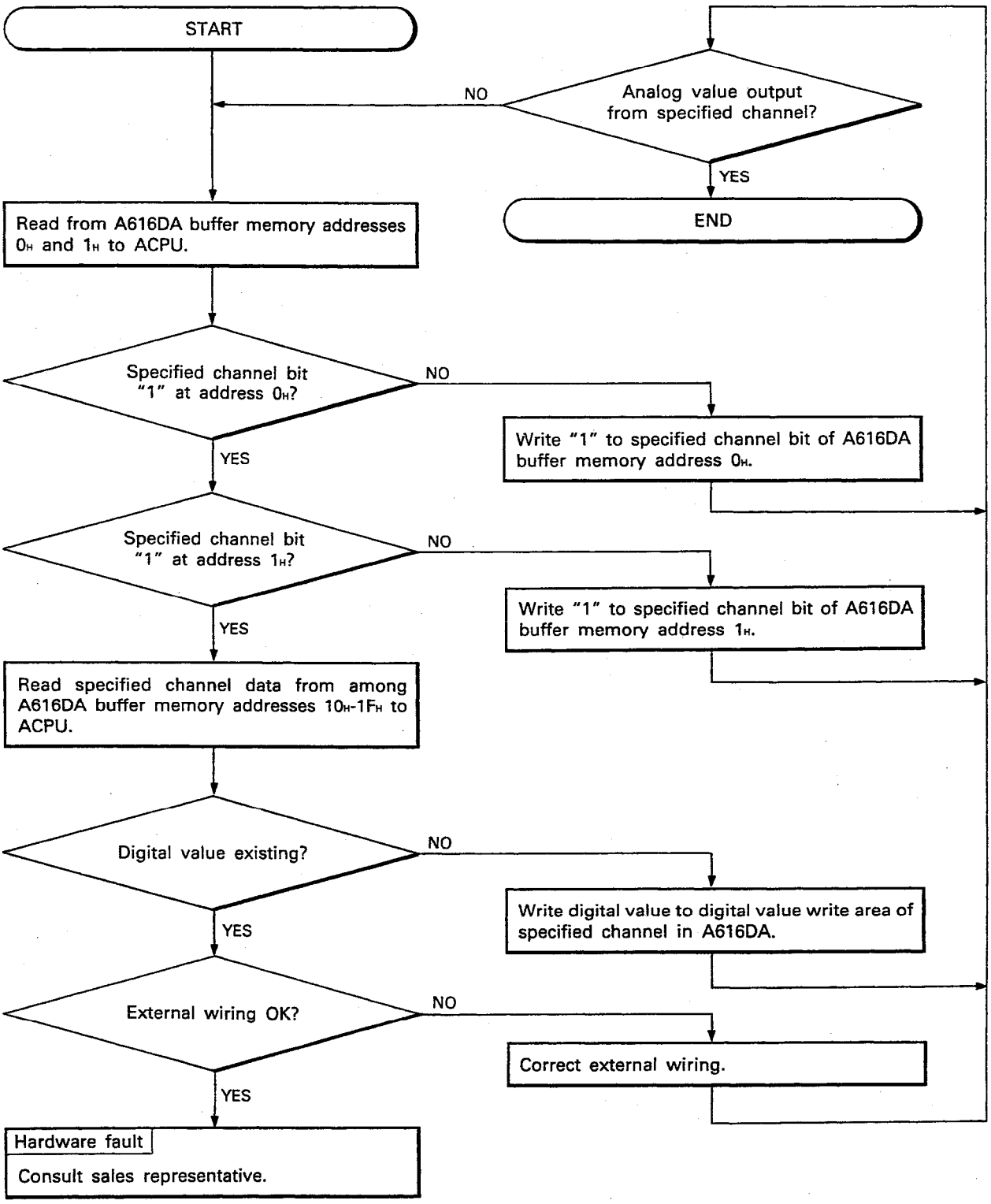
6. TROUBLESHOOTING

Basic troubleshooting procedures for the A616DA are given below. For information on the CPU module, see the corresponding CPU module User's Manual.

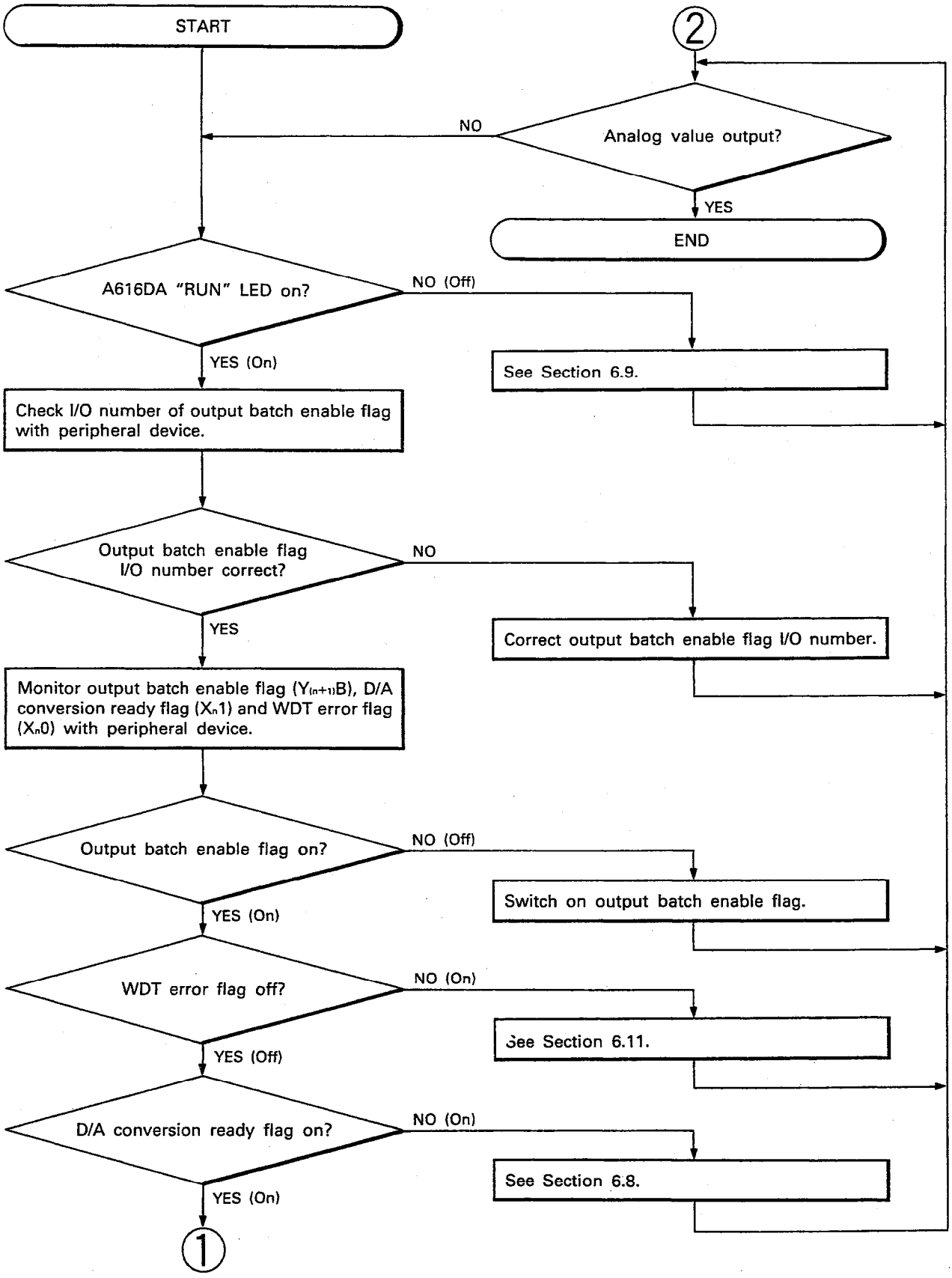
6.1 Symptoms

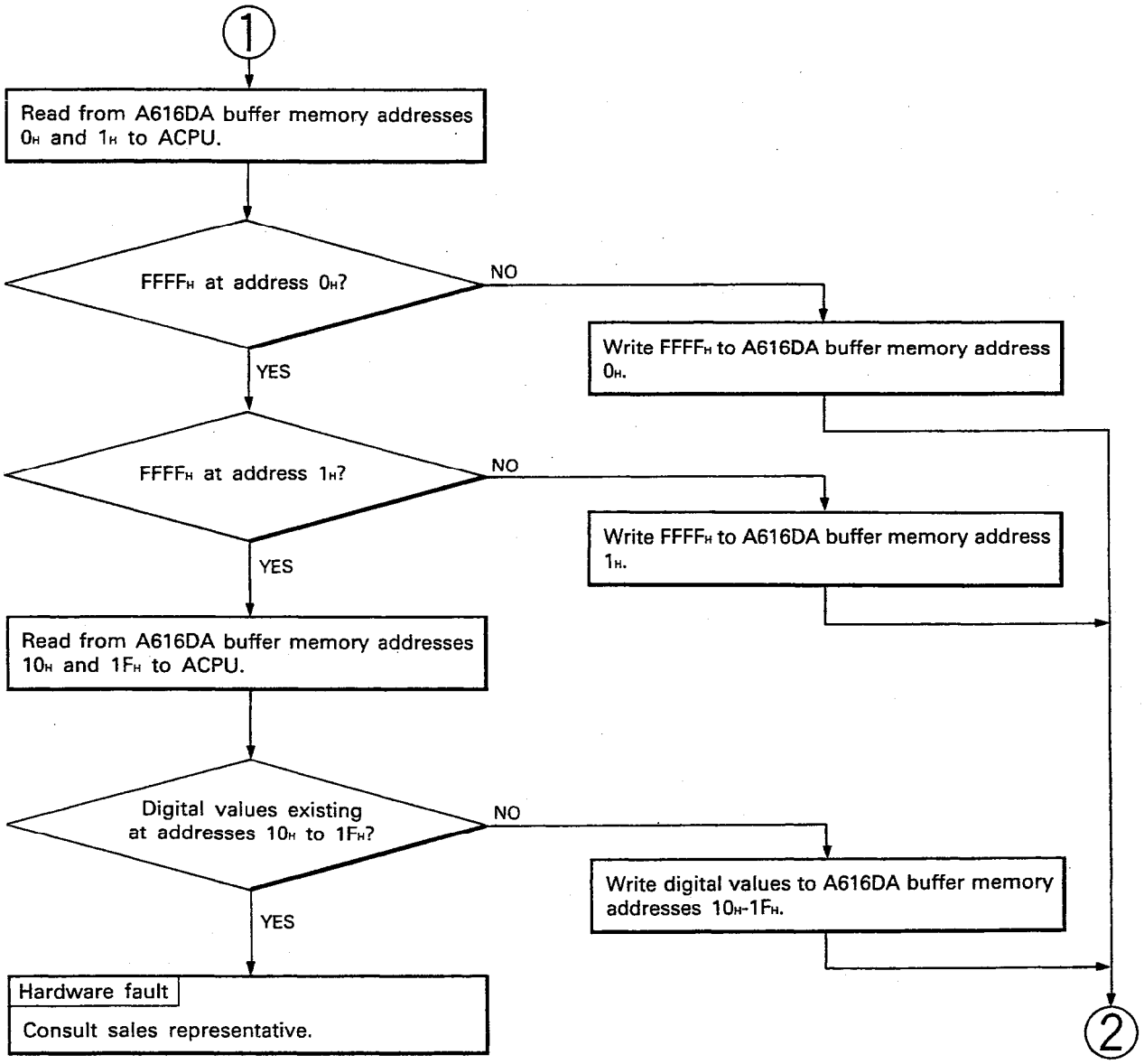
Symptom	Section
Analog value of only given channel is 0V.	Section 6.2
Analog values of all channels are 0V.	Section 6.3
Analog value of only given channel is offset value.	Section 6.4
Analog value of all channels are offset values.	Section 6.5
Analog value remains output at stop of ACPU.	Section 6.6
Analog value remains output with output batch enable flag ($Y_{(n+1)}B$) off.	Section 6.7
No correspondence between digital and analog values.	Section 6.8
A616DA "RUN" LED off.	Section 6.9
A616DA "RUN" LED flickering.	Section 6.10
A616DA WDT error flag (X_n0) on.	Section 6.11
D/A conversion ready flag (X_n1) remains off.	Section 6.12
A616DA error flag (X_n2) on.	Section 6.13

6.2 Analog Value of Only Given Channel is 0V

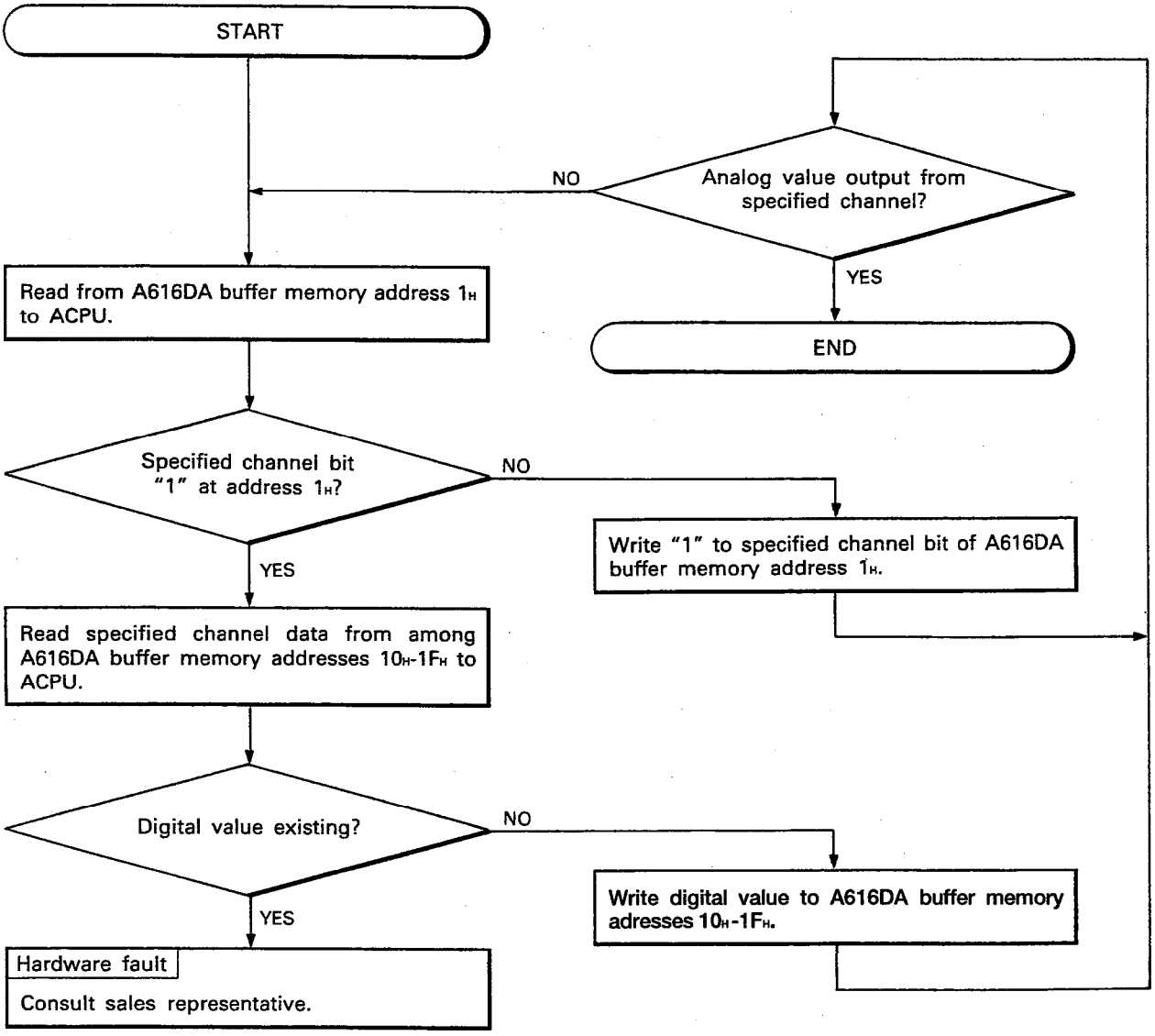


6.3 Analog Values of All Channels are 0V

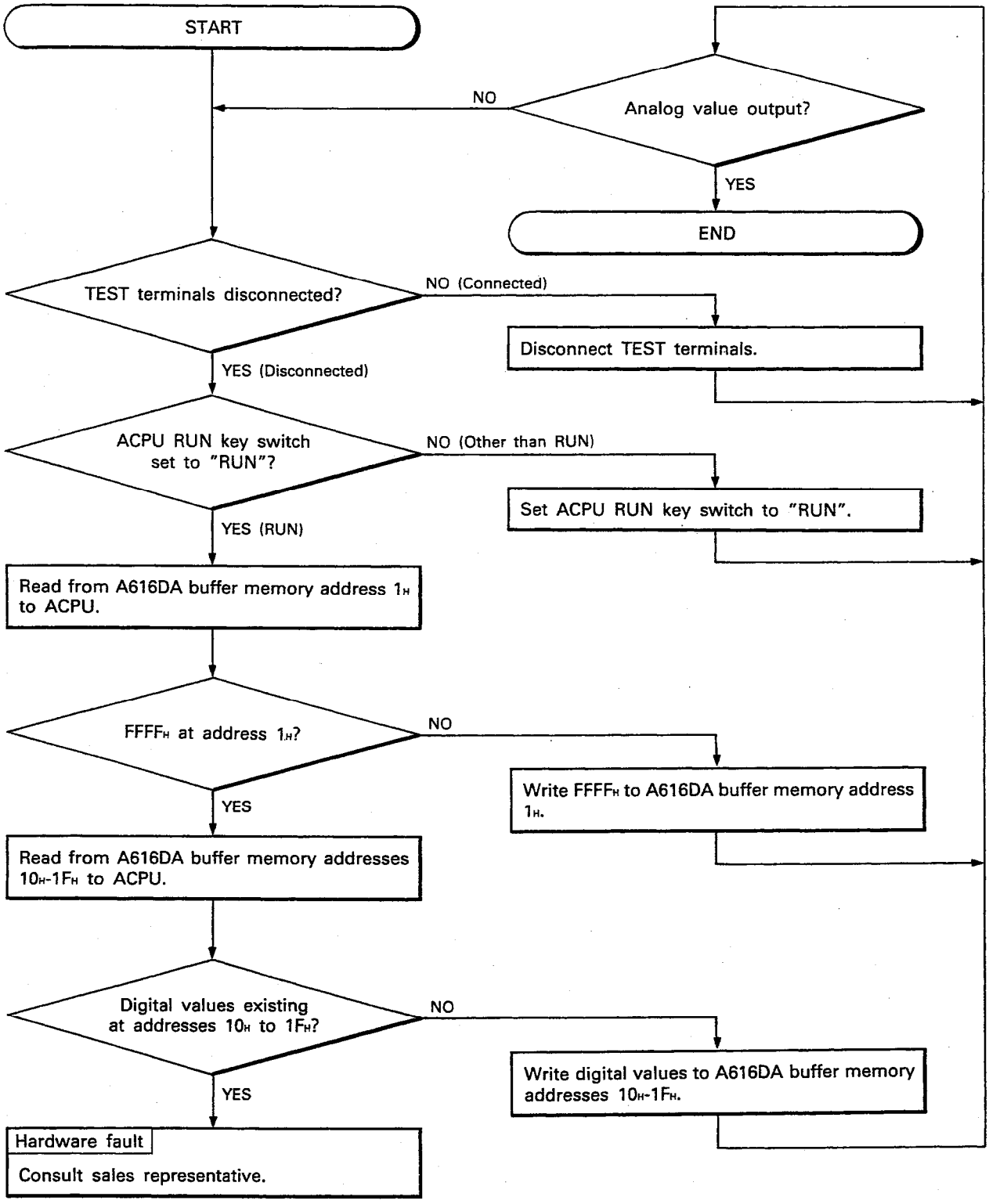



1
Read from A616DA buffer memory addresses 0H and 1H to ACPU.
FFFFH at address 0H?
NO
YES
Write FFFFH to A616DA buffer memory address 0H.
FFFFH at address 1H?
NO
YES
Write FFFFH to A616DA buffer memory address 1H.
Read from A616DA buffer memory addresses 10H and 1FH to ACPU.
Digital values existing at addresses 10H to 1FH?
NO
YES
Write digital values to A616DA buffer memory addresses 10H-1FH.
Hardware fault
Consult sales representative.
2

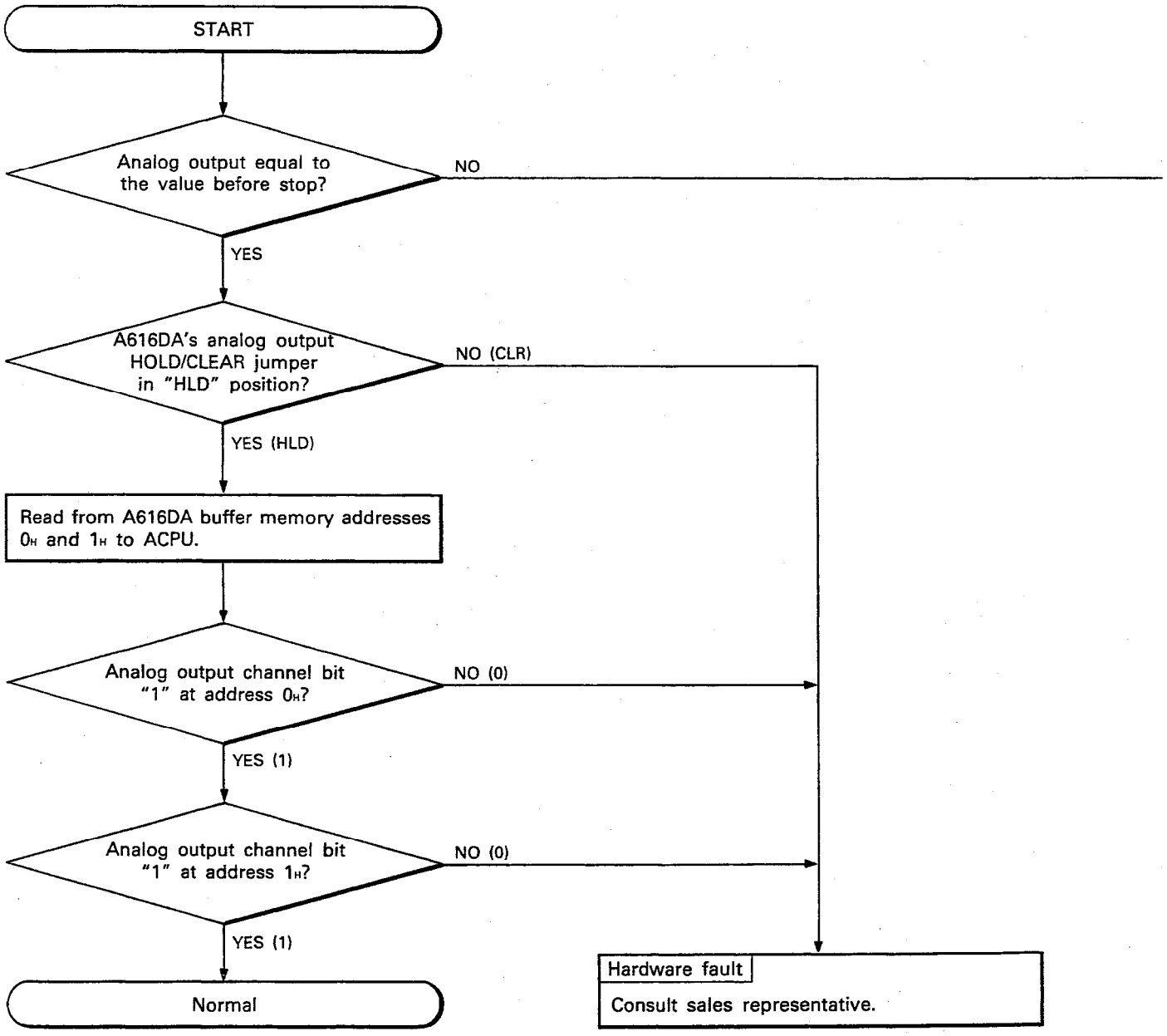
6.4 Analog Value of Only Given Channel is Offset Value

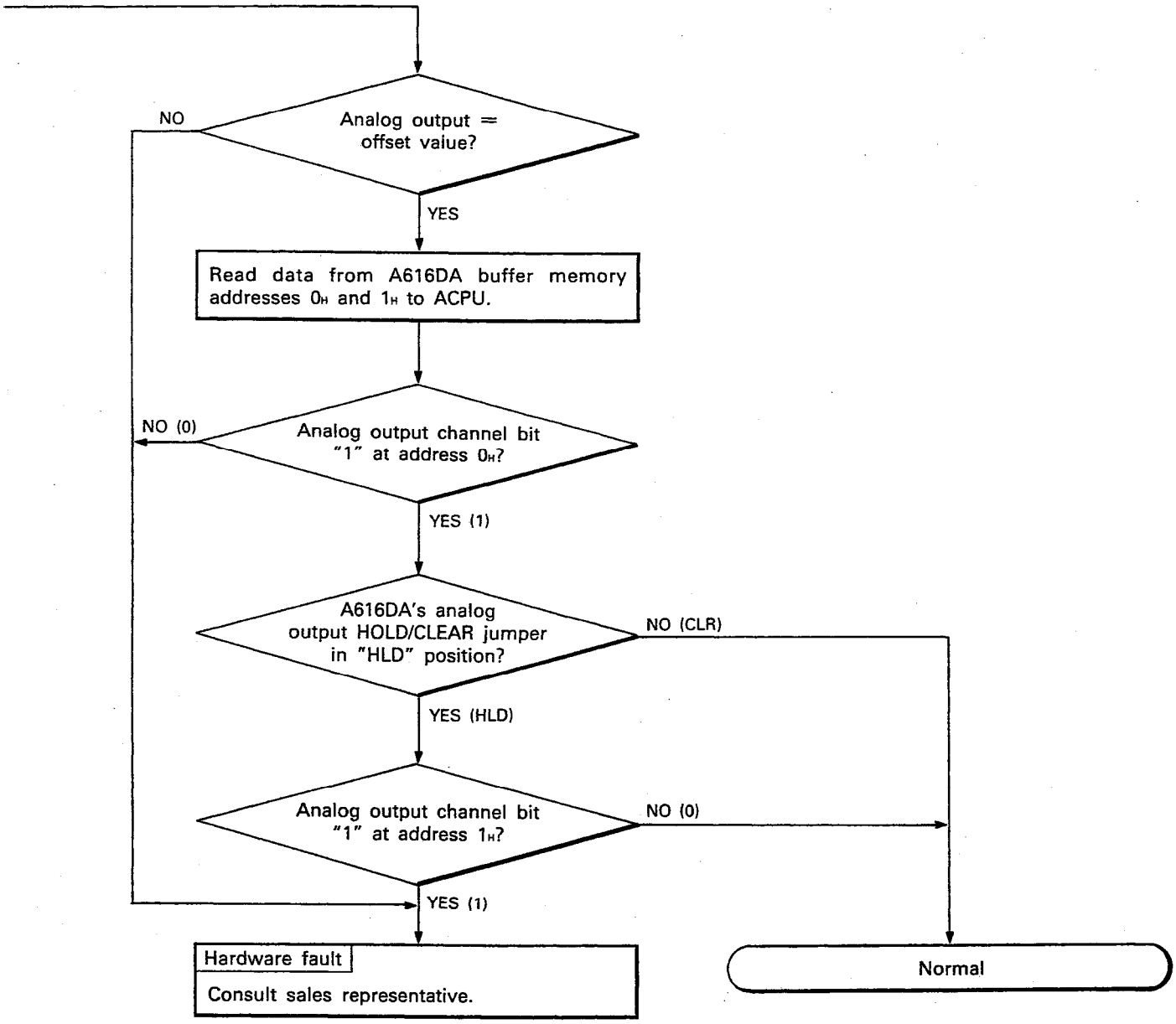


6.5 Analog Values of All Channels are Offset Values

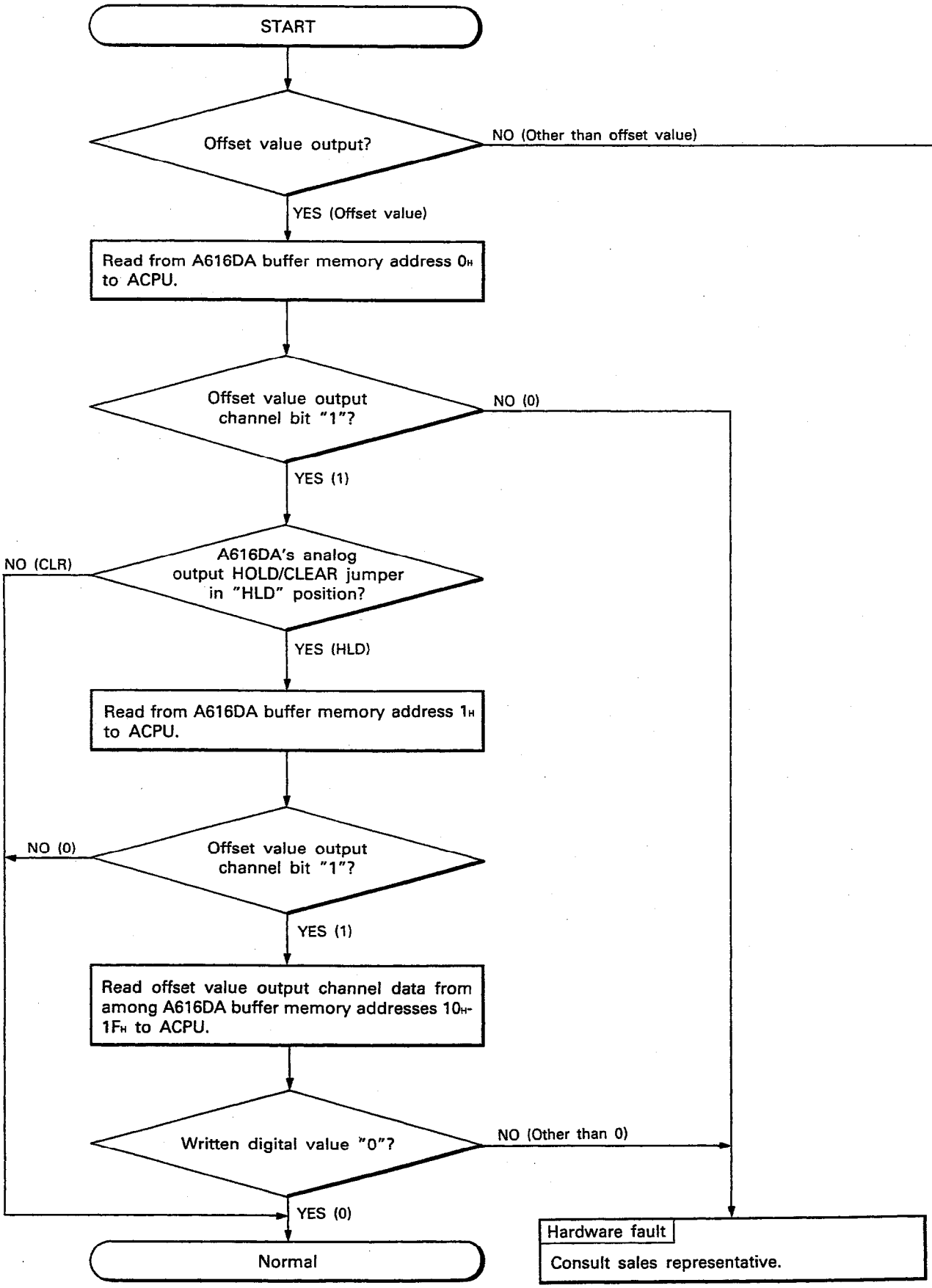


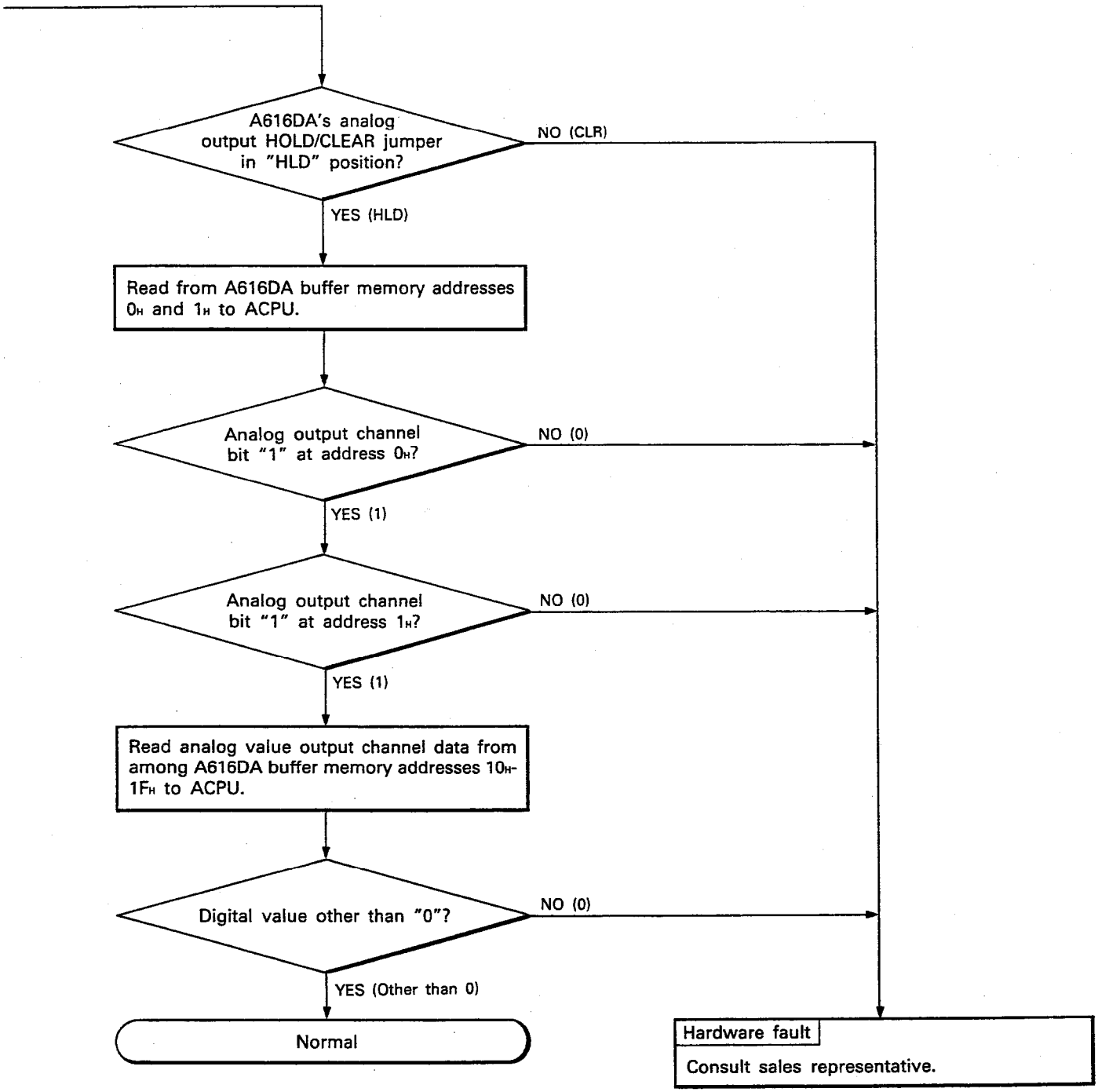
6.6 Analog Value Remains Output at Stop of ACPU



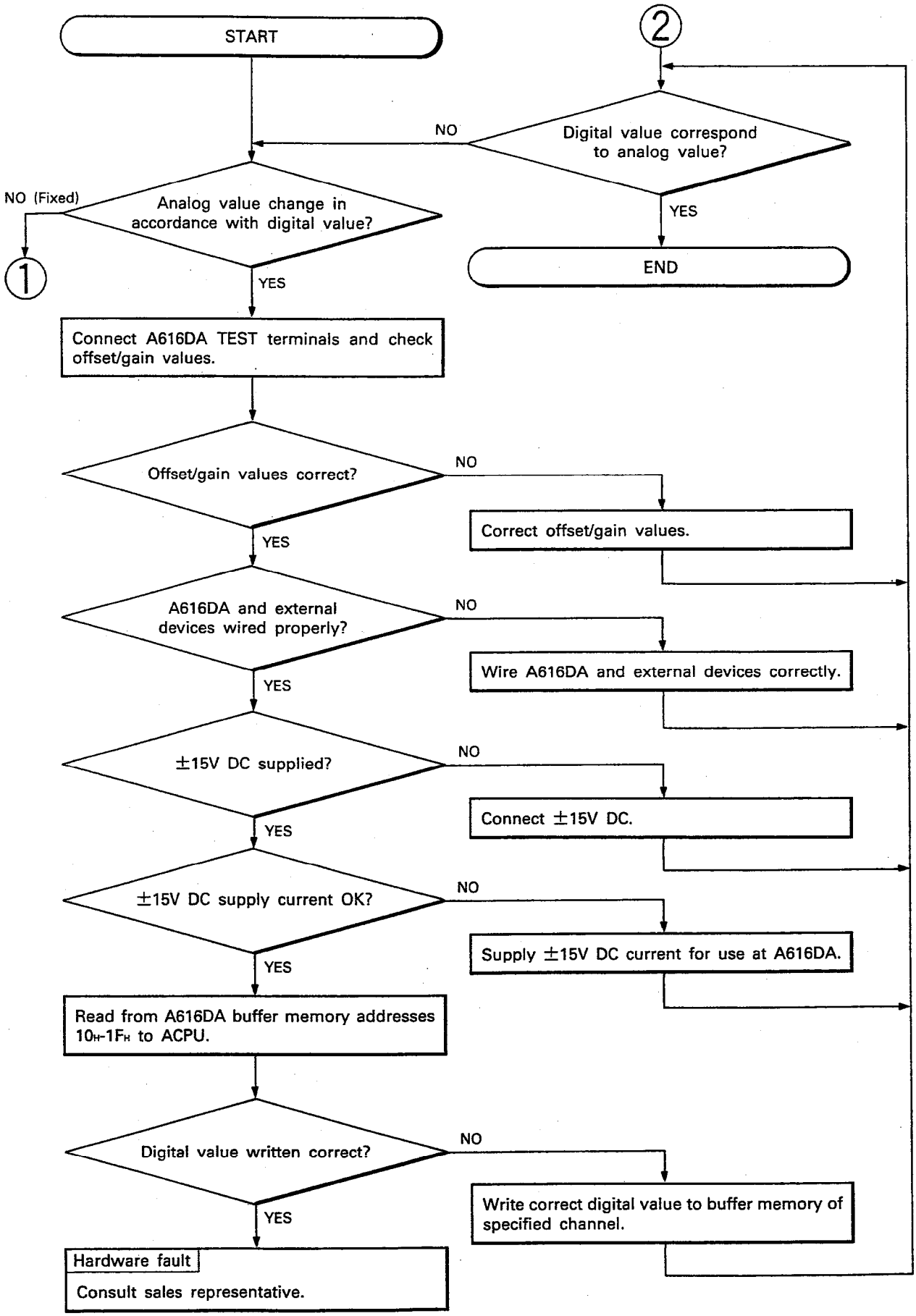

NO
Analog output = offset value?
YES
Read data from A616DA buffer memory addresses 0H and 1H to ACPU.
NO (0)
Analog output channel bit "1" at address 0H?
YES (1)
A616DA's analog output HOLD/CLEAR jumper in "HLD" position?
NO (CLR)
YES (HLD)
Analog output channel bit "1" at address 1H?
NO (0)
YES (1)
Hardware fault
Consult sales representative.
Normal

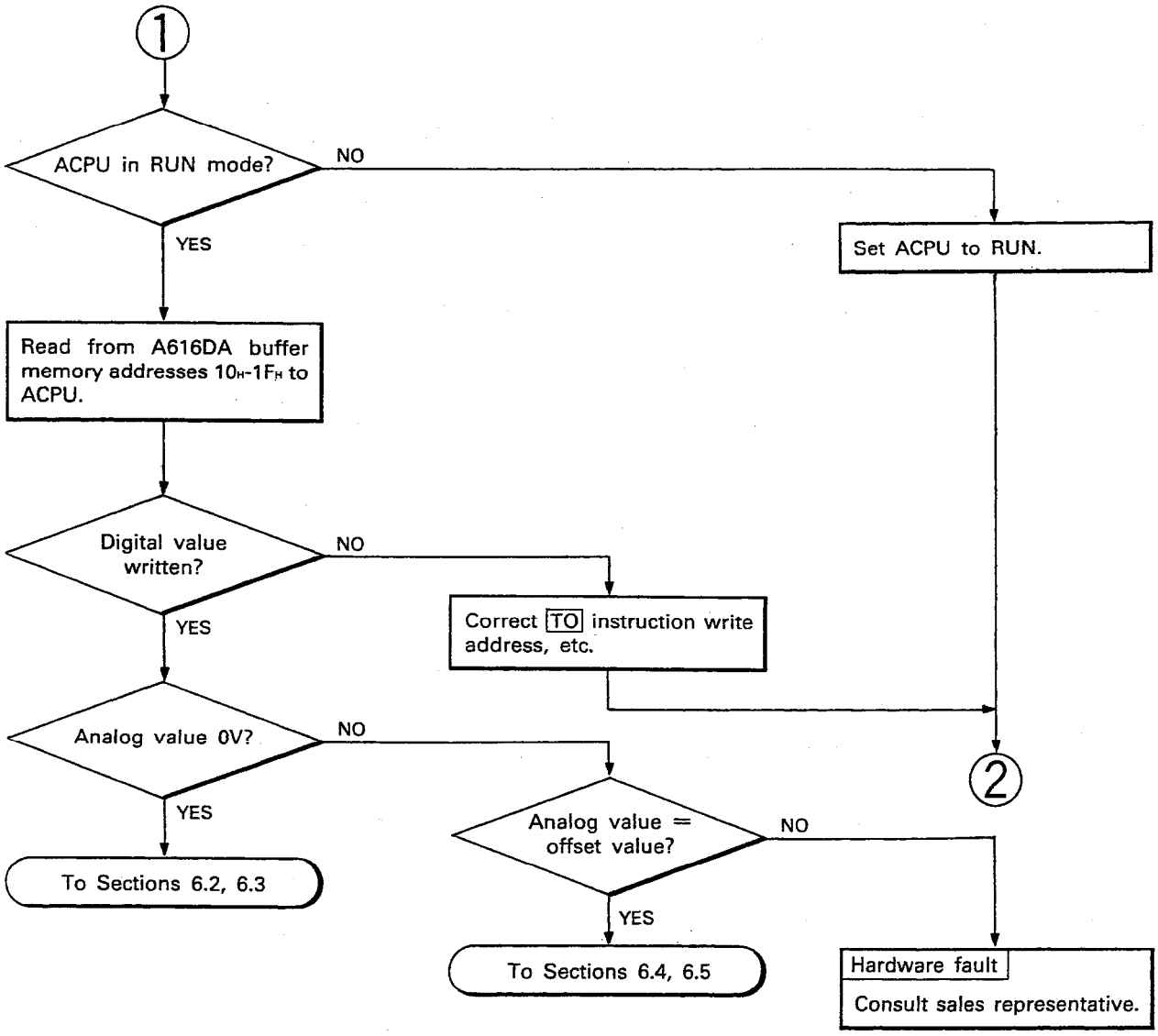
6.7 Analog Value Remains Output with Output Batch Enable Flag ($Y_{(n+1)}B$) Off



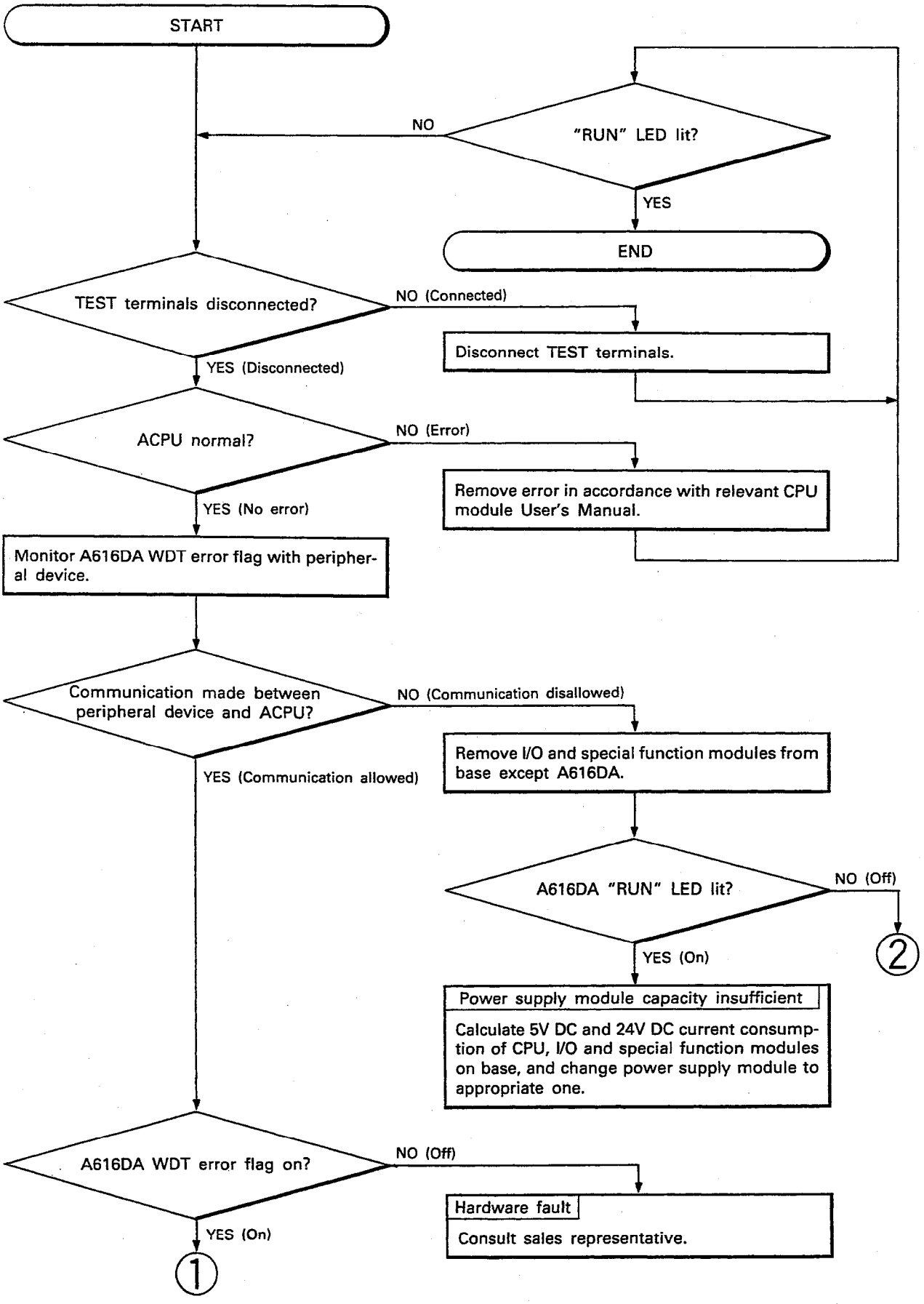

A616DA's analog output HOLD/CLEAR jumper in "HLD" position?
NO (CLR)
YES (HLD)
Read from A616DA buffer memory addresses 0H and 1H to ACPU.
Analog output channel bit "1" at address 0H?
NO (0)
YES (1)
Analog output channel bit "1" at address 1H?
NO (0)
YES (1)
Read analog value output channel data from among A616DA buffer memory addresses 10H-1FH to ACPU.
Digital value other than "0"?
NO (0)
YES (Other than 0)
Normal
Hardware fault
Consult sales representative.

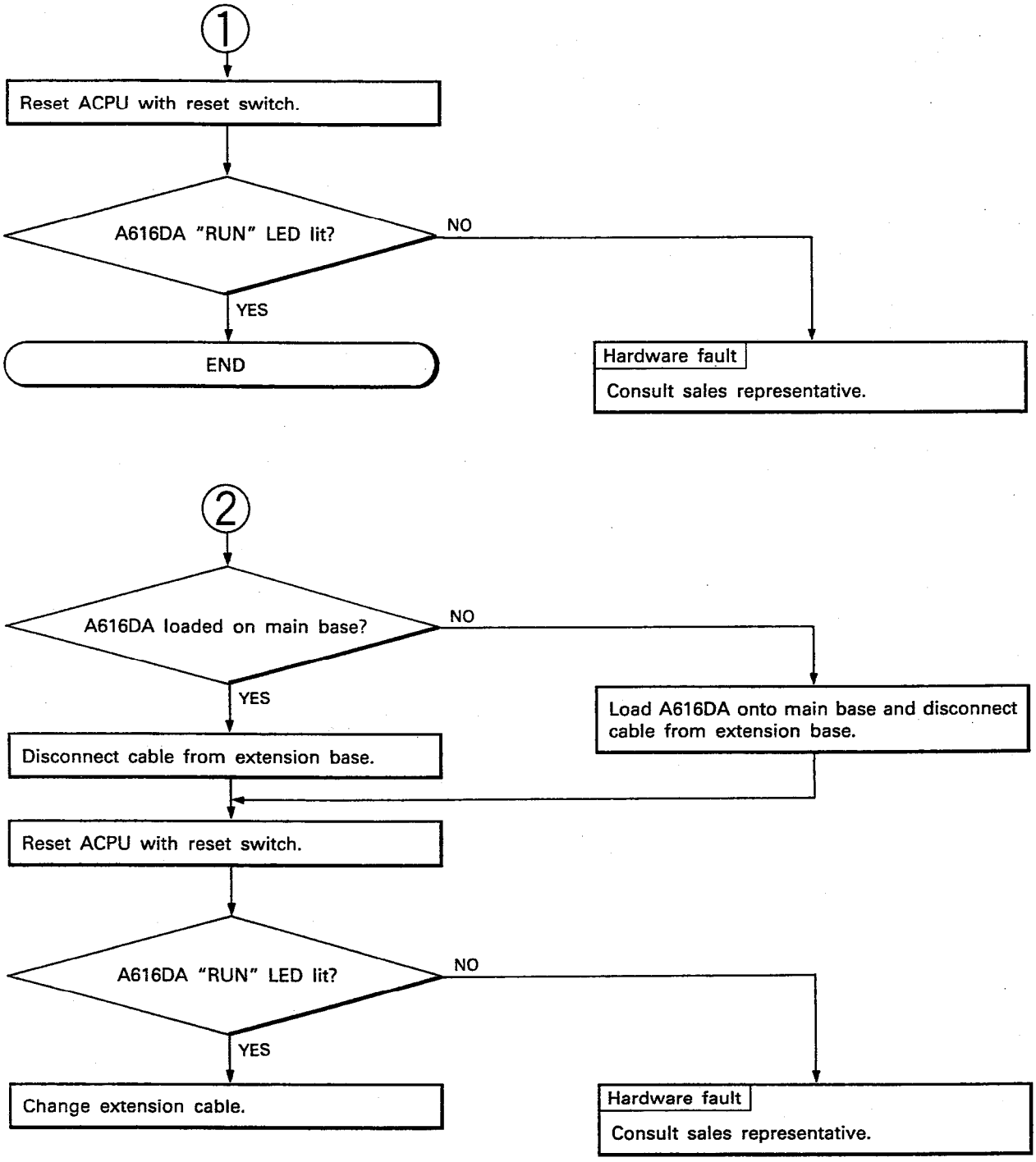
6.8 No Correspondence between Digital and Analog Values



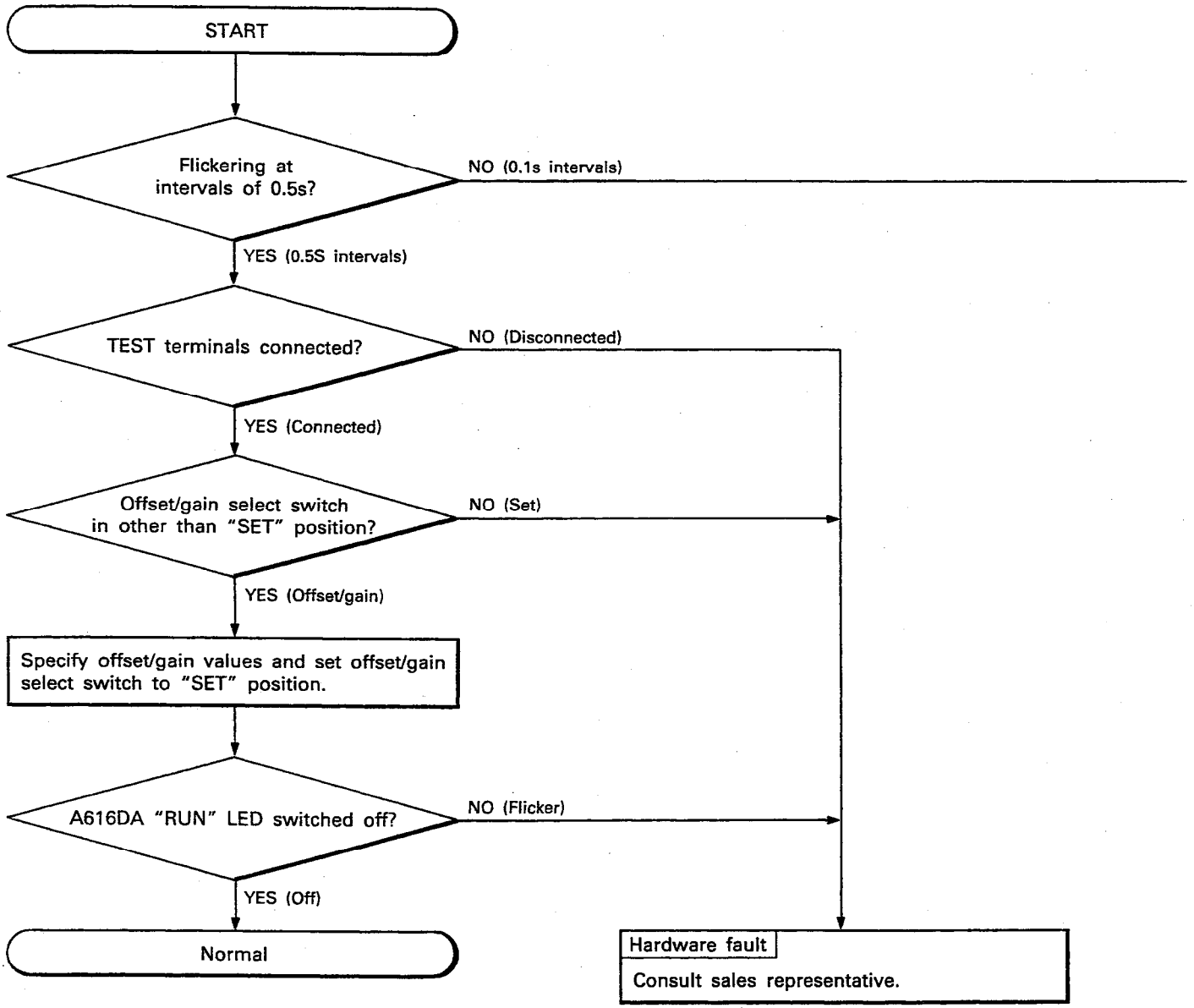

1
ACPU in RUN mode?
NO
YES
Set ACPU to RUN.
Read from A616DA buffer memory addresses 10H-1FH to ACPU.
Digital value written?
NO
YES
Correct TO instruction write address, etc.
Analog value 0V?
NO
YES
2
Analog value = offset value?
NO
YES
To Sections 6.2, 6.3
To Sections 6.4, 6.5
Hardware fault
Consult sales representative.

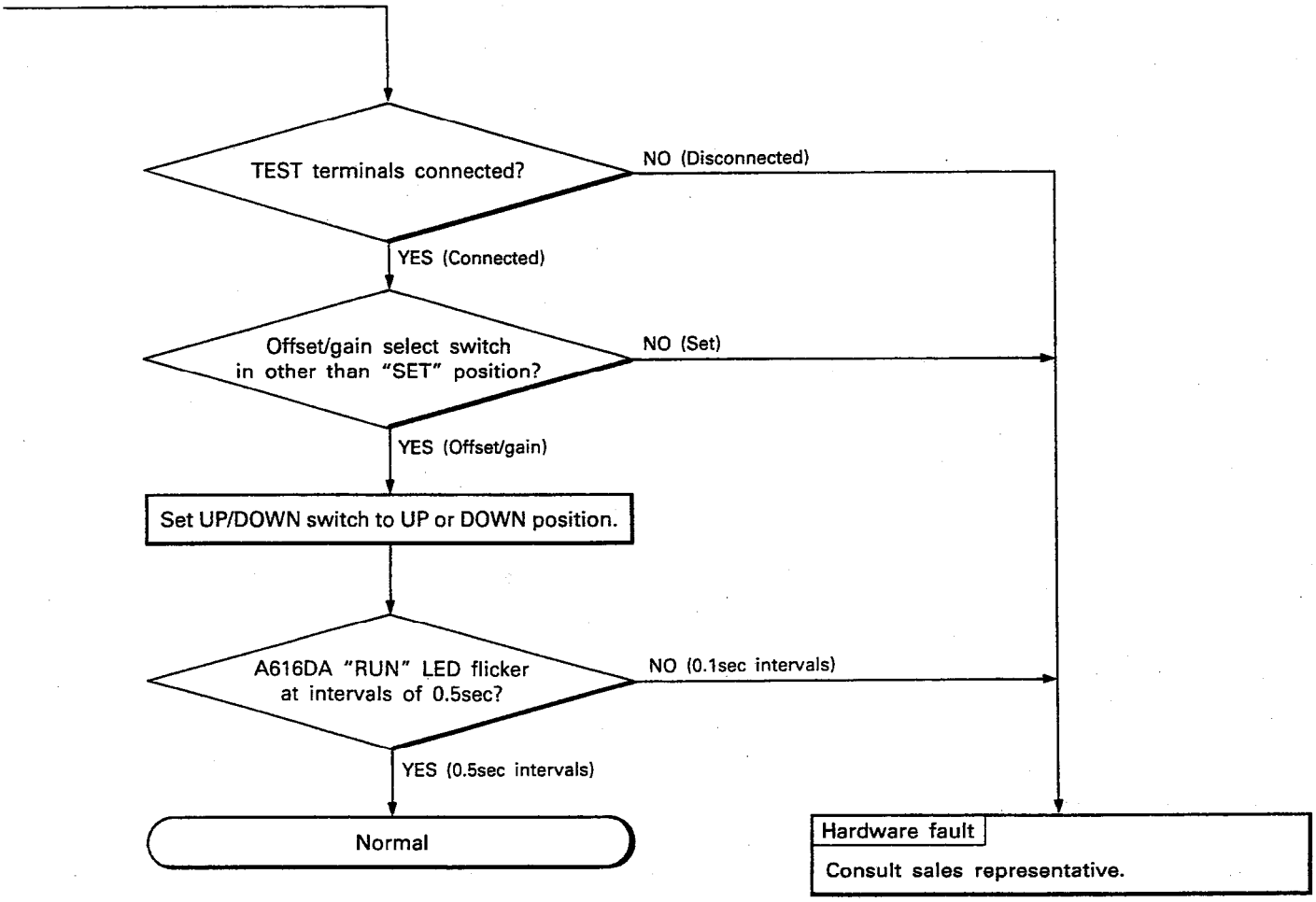
6.9 A616DA "RUN" LED Off



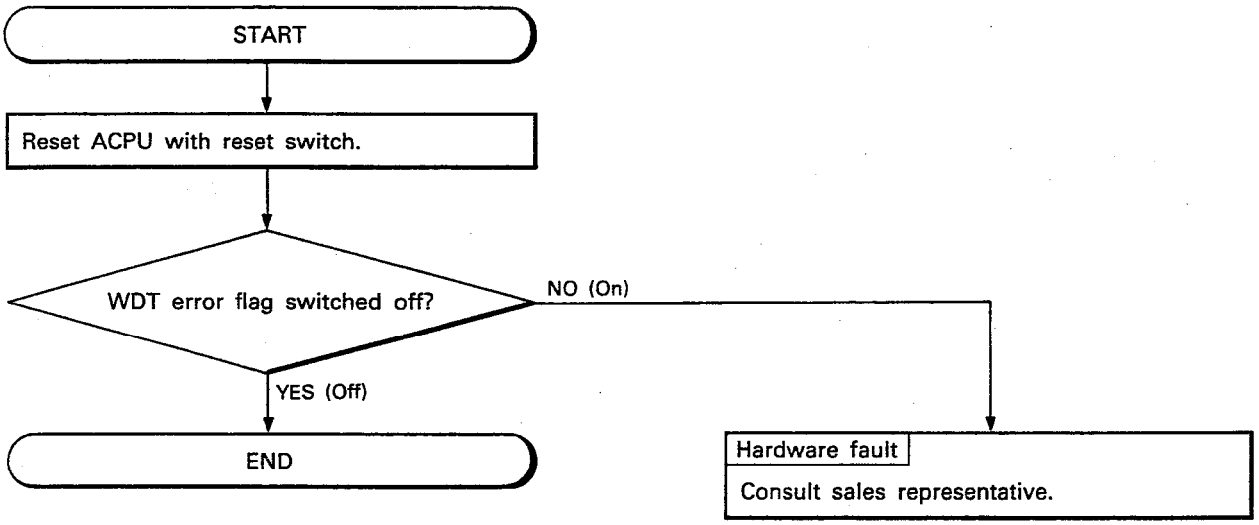

①
Reset ACPU with reset switch.
A616DA "RUN" LED lit?
NO
YES
END
Hardware fault
Consult sales representative.
②
A616DA loaded on main base?
NO
YES
Load A616DA onto main base and disconnect cable from extension base.
Disconnect cable from extension base.
Reset ACPU with reset switch.
A616DA "RUN" LED lit?
NO
YES
Change extension cable.
Hardware fault
Consult sales representative.

6.10 A616DA "RUN" LED Flickering

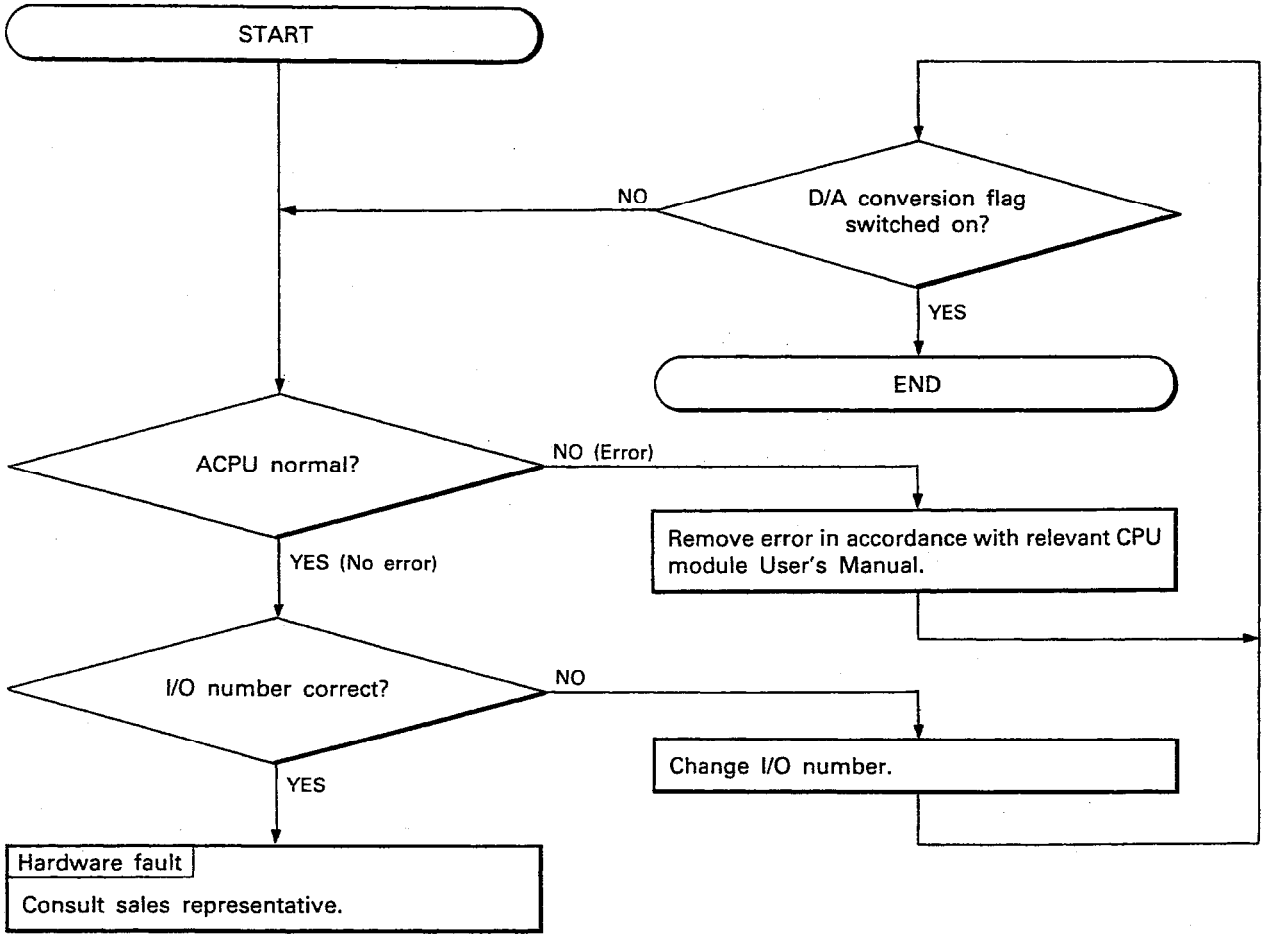



TEST terminals connected?
NO (Disconnected)
YES (Connected)
Offset/gain select switch in other than "SET" position?
NO (Set)
YES (Offset/gain)
Set UP/DOWN switch to UP or DOWN position.
A616DA "RUN" LED flicker at intervals of 0.5sec?
NO (0.1sec intervals)
YES (0.5sec intervals)
Normal
Hardware fault
Consult sales representative.

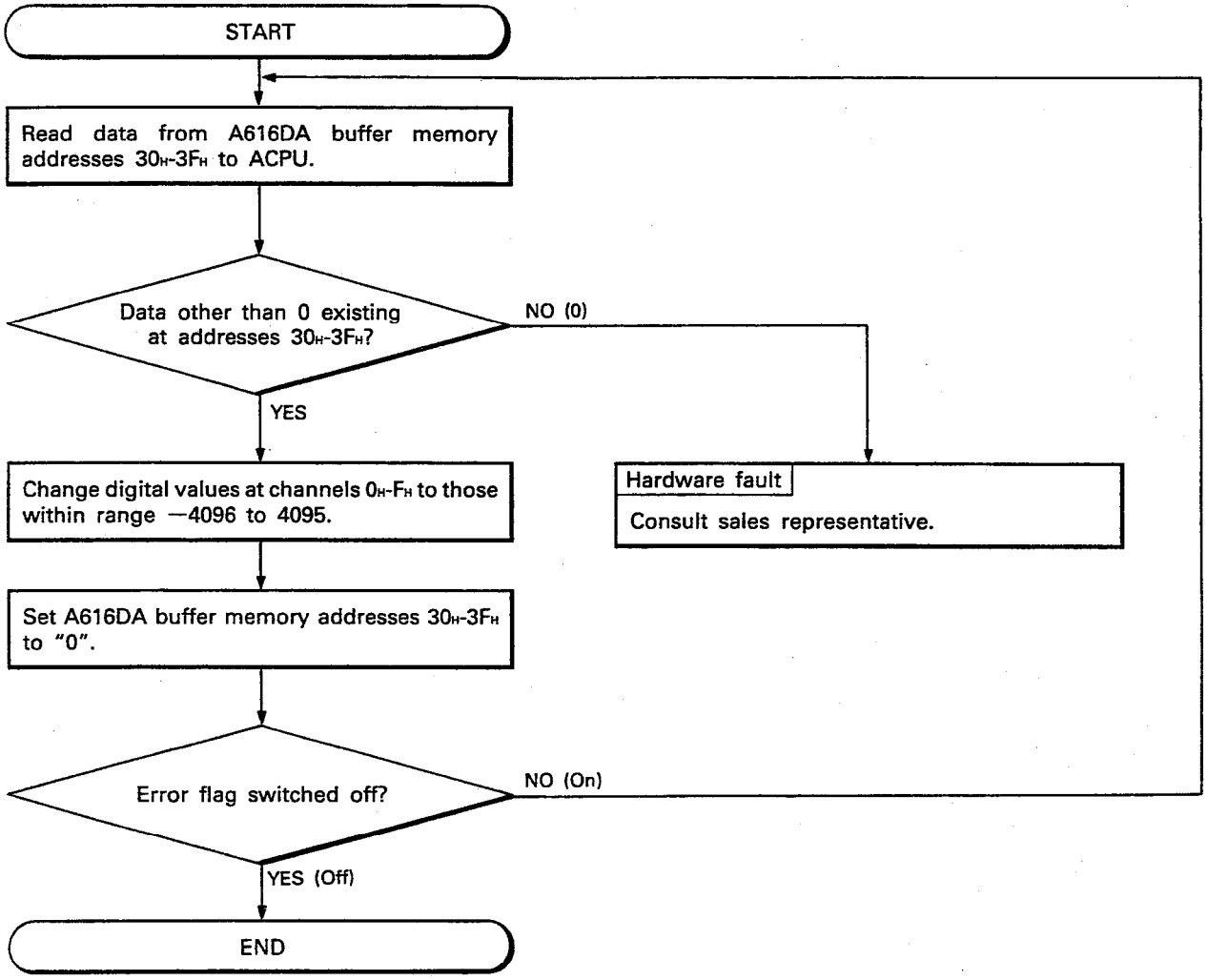
6.11 A616DA WDT Error Flag (X.0) On



6.12 D/A Conversion Ready Flag (X□1) Remains Off

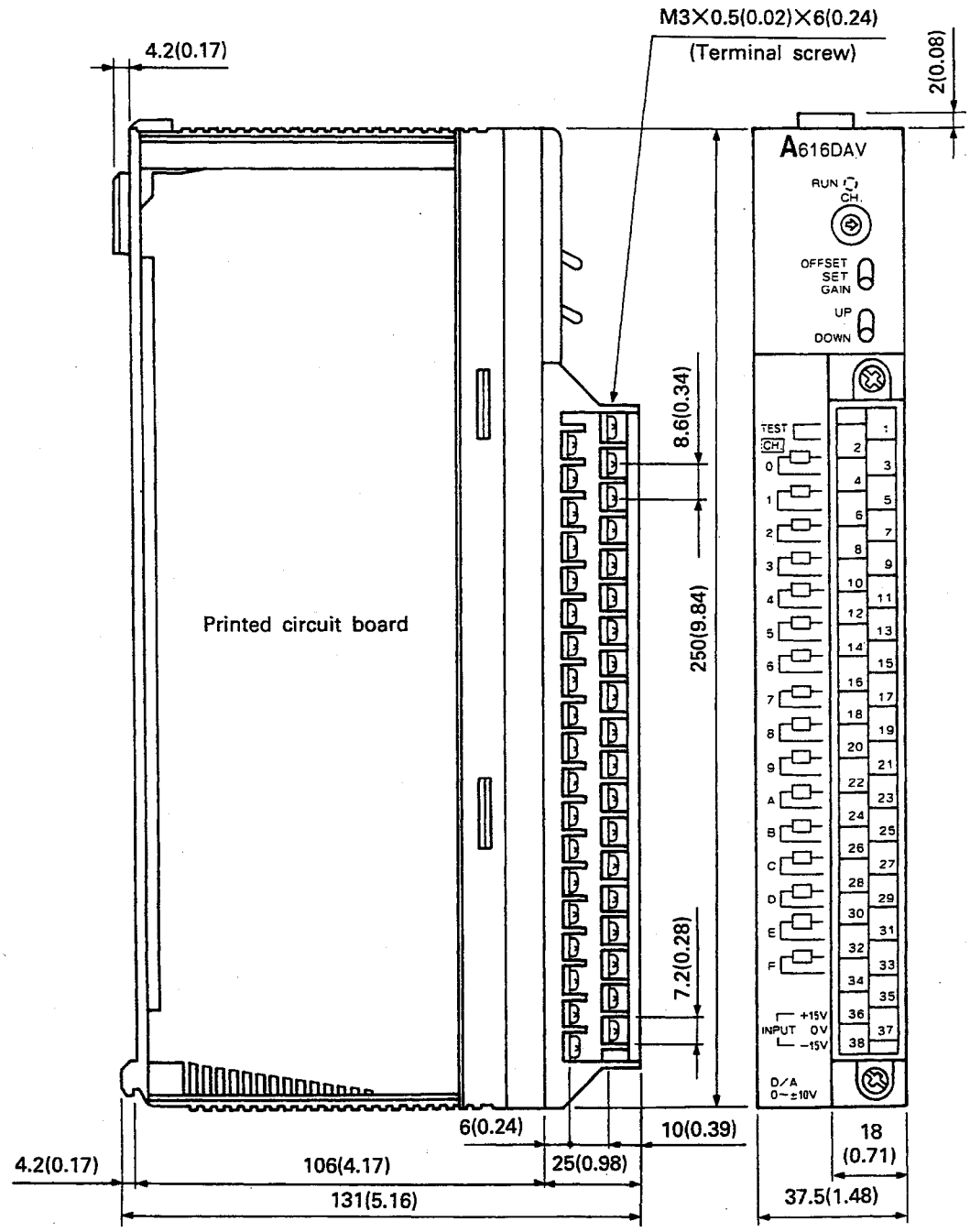


6.13 A616DA Error Flag (X□2) On



APPENDICES

APPENDIX 1 Dimensions (A616DAV)



Unit: mm(inch)

APPENDIX 2 Program Examples for Compact Type CPU

POINT

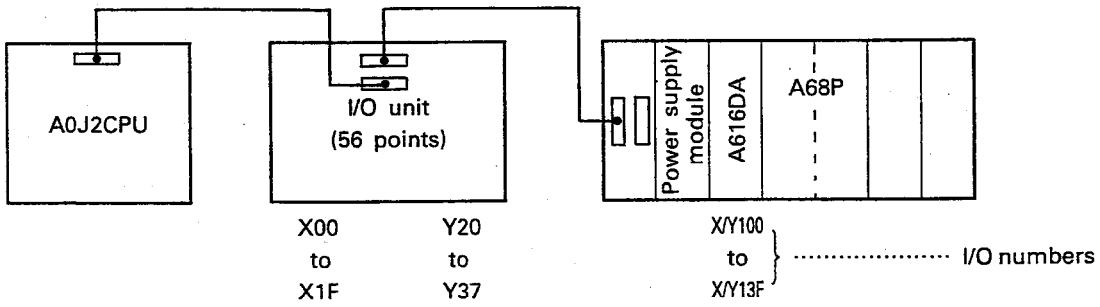
(1) When the A0J2 is connected to an extension base, one slot of the extension base is 64 points.

(2) When the A616DA is loaded in the extension base, the first 32 points may only be used.

2.1 Digital value setting program

The following program writes a value (0 to 4000) defined by the BCD digital switch to channels 0 to 3 of the A616DA.
(This program includes a program for disabling channels 4 to F for D/A conversion and analog output.)

【Module arrangement】



【Specifications】

(1) Executed commands

(a) D/A conversion disable channel setting command ····· X0

(b) Analog output disable channel setting command ····· X1

(c) Digital value setting commands
1) Channel 0 ····· X2
2) Channel 1 ····· X3
3) Channel 2 ····· X4
4) Channel 3 ····· X5

(2) Digital value setting (4 BCD digits) ····· X10 to X1F

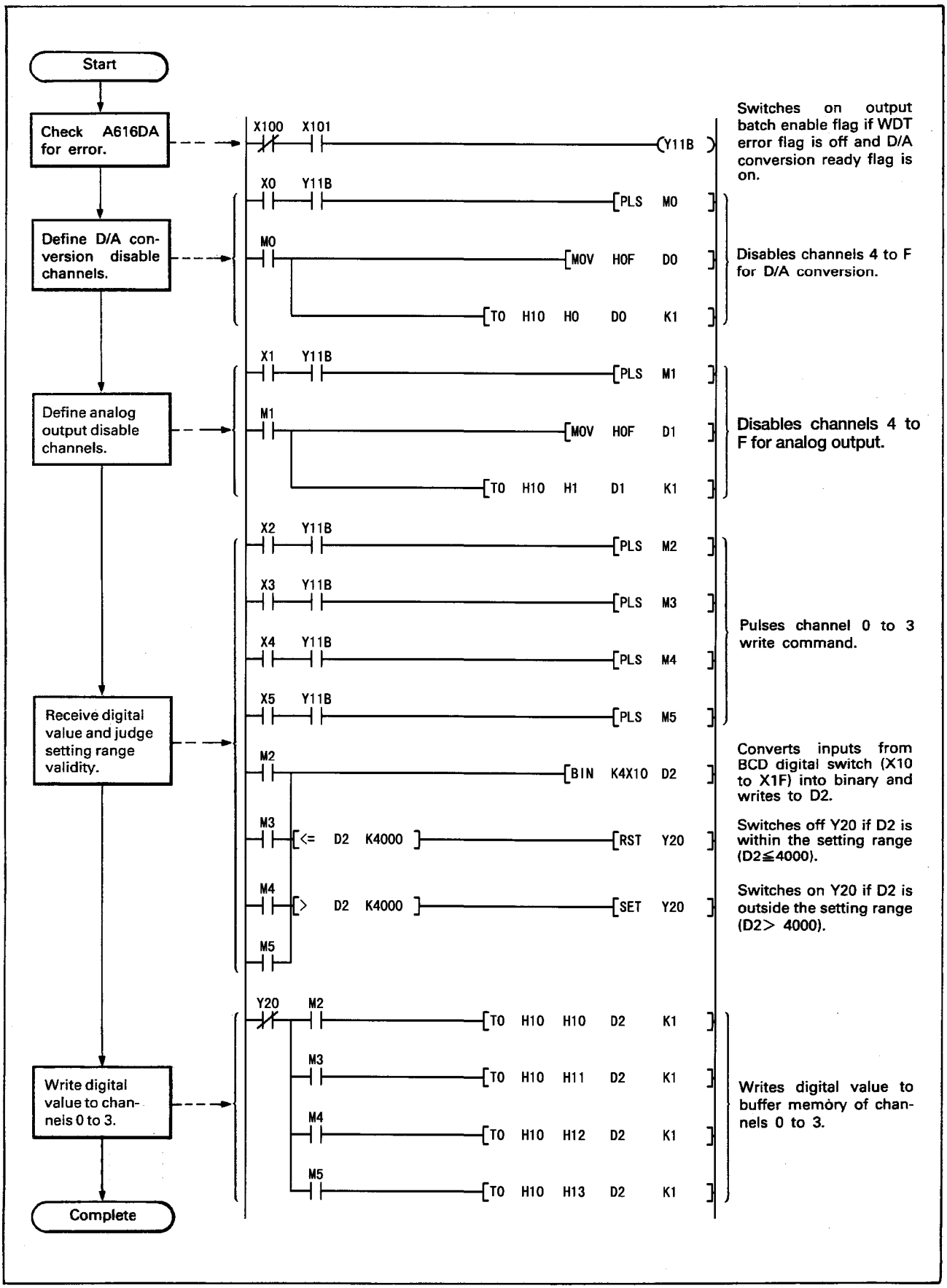
(3) Digital value setting error output ····· Y20

(4) Register for storing D/A conversion disable channel ····· D0

(5) Register for storing digital value ····· D1

(6) Register for storing digital value ····· D2

【Program example】



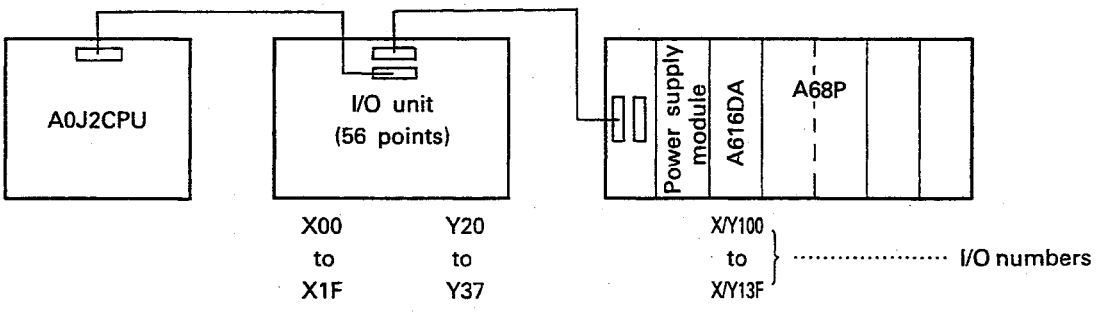
2.2 Digital value setting error detection program

The following program detects any digital value outside the range —4096 to 4095 and outputs the corresponding channel to Y30-Y37 in BCD.

Example

1) Channel 0 ····· 1 output to Y30-Y37.
2) Channel F ····· 16 output to Y30-Y37.

【Module arrangement】



【Specifications】

(1) Executed commands

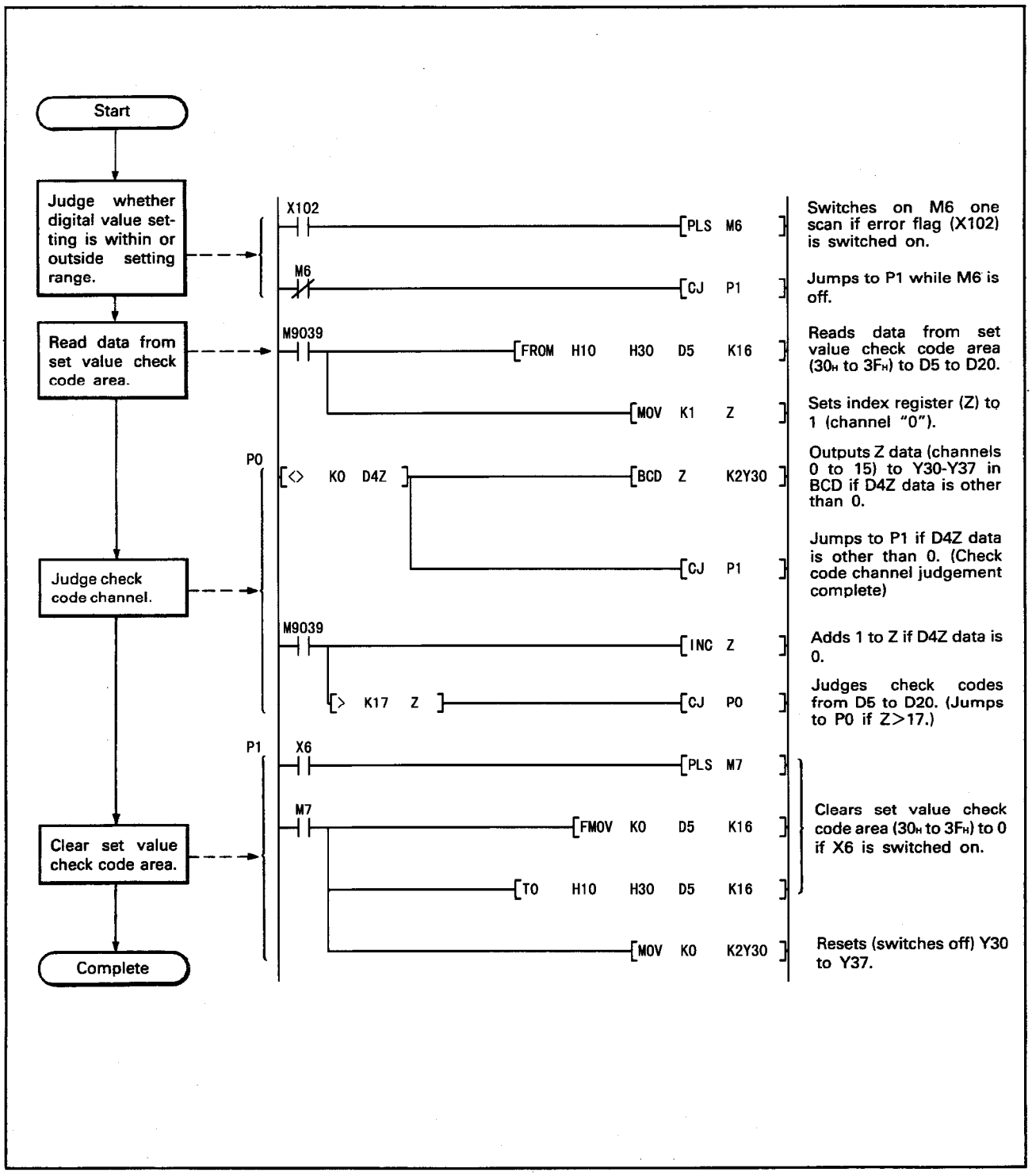
(a) Judgement of digital value defined outside the setting range ····· X102 (error flag)

(b) Error flag off command ····· X6

(c) Check code register judgement command ····· M6

(2) Registers for storing set value
check code area data ····· D5 to D20

【Program example】



APPENDIX 3 A68P Power Supply Module

3.1 Specifications

Item		Specifications
		A68P
Location in base unit		I/O module slot
Number of points occupied		2 slots occupied, 1 slot 16 points
Input voltage		100 to 120V AC $^{+10\%}_{-15\%}$ (85 to 132V AC)
		200 to 240V AC $^{+10\%}_{-15\%}$ (170 to 264V AC)
Input frequency		50/60Hz ± 5%
Max. input apparent power		95VA
Inrush current		20A, within 8ms
Rated output current	+15V DC	1.2A
	−15V DC	0.7A
*1 Overcurrent protection	+15V DC	1.64A or higher
	−15V DC	0.94A or higher
Efficiency		65% or higher
Power indicator		Power LED display
Power ON monitor output		Contact output
		Switched on if +15V DC output is +14.25V or higher or −15V DC output is −14.25V or lower.
		Min. contact switching load: 5V DC, 10mA Max. contact switching load: 264V AC, 2A (R load)
Terminal screw size		M3 × 0.5(0.02) × 6(0.24)
Wire size		0.75 to 2mm^2 (18 to 14 AWG)
Solderless terminal		V1.25—4, V1.25—YS4A, V2—S4, V2—YS4A
Tightening torque		68N·cm
External dimensions mm(inch)		250(9.84) × 75.5(2.97) × 121(4.76)
Weight kg(lb)		0.9(1.98)

Table 3.1 A68 Specifications

POINT

*1: Overcurrent protection

The overcurrent protection shuts off the +15V DC circuit if a current higher than the specified value flows in the circuit and:

(a) Both +15V DC and −15V DC are switched off if overcurrent has occurred at +15V; or

(b) −15V DC is switched off but +15V remains output if overcurrent has occurred at −15V; and

(c) The power supply module LED is switched off or dimly lit due to 15V DC voltage drop.

If this protection has been activated, remote the overcurrent factor (e.g. insufficient current capacity, short) and start up the system.

3.2 Handling

3.2.1 Handling instructions

(1) Protect the power supply module and its terminal block and pin connectors from impact loads.

(2) Do not remove the printed circuit boards from the housing. There are no user-serviceable parts on the boards.

(3) Ensure that no conductive debris can enter the module. If it does, make sure that it is removed. Guard particularly against wire offcuts.

(4) Tighten the screws as specified below:

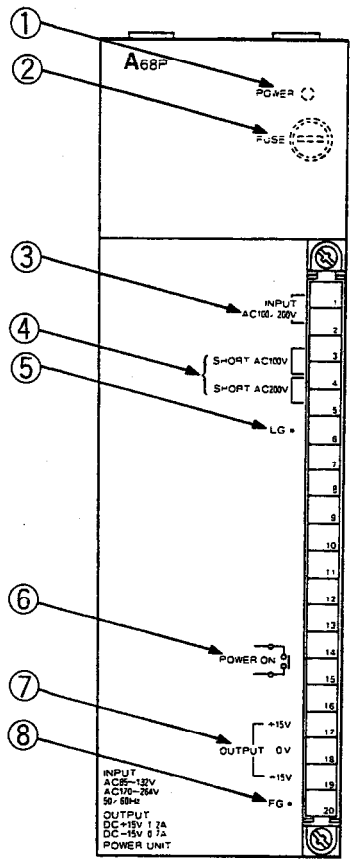
Screw	Tightening Torque Rang N·cm
Power supply module terminal screw (M3 screw)	39 to 59
Module installation screw (optional) (M4 screw)	78 to 118

(5) To load the module onto the base, press the module against the base so that the catch on the top of the unit is securely locked. To unload the module, push the catch, and after the catch is disengaged from the base, pull the module toward you.

3.2.2 Using instruction

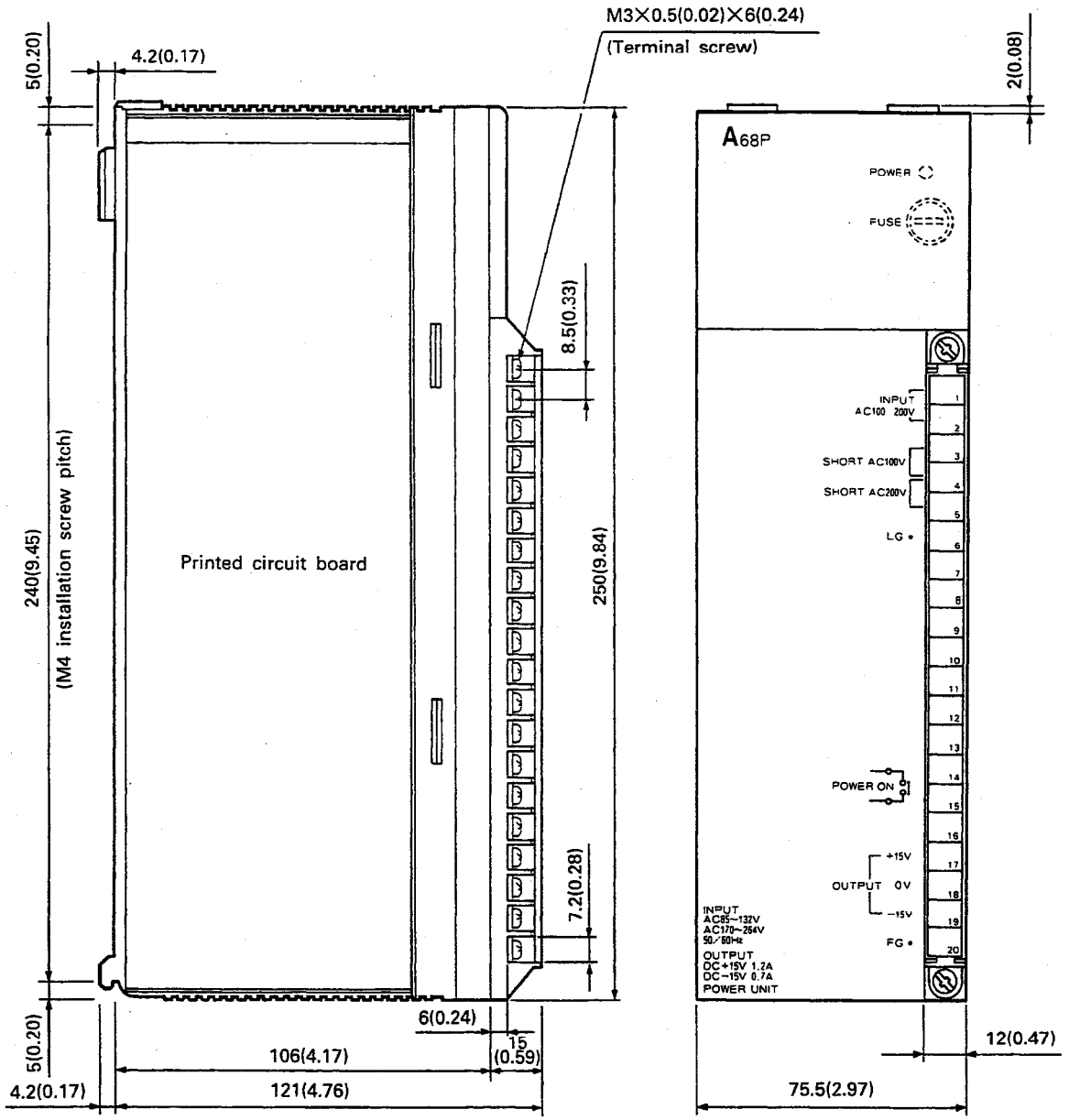
(1) When the A68P is used, connect the LG and FG terminals if FG is not grounded.

3.2.3 Nomenclature



No.	Description	Explanation
①	"POWER" LED	• LED for indicating ±15 V DC power.
②	Power fuse assembly	• 4A cartridge fuse for AC input power fitted in fuse holder.
③	Power input terminals	• Power input terminals for 100 or 200V AC.
④	Input voltage select terminals	• The input voltage must be specified with a jumper. • When using the 100V range, connect the jumper across the "SHORT AC100V" terminals. • When using the 200V range, connect the jumper across the "SHORT AC200V" terminals.
⑤	LG terminal	• Power filter ground. • Outputs half the power supply voltage.
⑥	Power ON monitor contacts	• Normally closed when the power supply is operating normally and giving ± 15V DC output.
⑦	+15V, 0V, −15V terminals	• ±15V DC output supplied to appropriate module externally.
⑧	FG terminal	• Connected to printed circuit board shielding pattern.

3.3 Dimensions



Unit: mm(inch)

MEMO

WARRANTY

Please confirm the following product warranty details before using this product.

1. Gratis Warranty Term and Gratis Warranty Range

If any faults or defects (hereinafter "Failure") found to be the responsibility of Mitsubishi occurs during use of the product within the gratis warranty term, the product shall be repaired at no cost via the sales representative or Mitsubishi Service Company.
However, if repairs are required onsite at domestic or overseas location, expenses to send an engineer will be solely at the customer's discretion. Mitsubishi shall not be held responsible for any re-commissioning, maintenance, or testing on-site that involves replacement of the failed module.

[Gratis Warranty Term]

The gratis warranty term of the product shall be for one year after the date of purchase or delivery to a designated place.
Note that after manufacture and shipment from Mitsubishi, the maximum distribution period shall be six (6) months, and the longest gratis warranty term after manufacturing shall be eighteen (18) months. The gratis warranty term of repair parts shall not exceed the gratis warranty term before repairs.

[Gratis Warranty Range]

(1) The range shall be limited to normal use within the usage state, usage methods and usage environment, etc., which follow the conditions and precautions, etc., given in the instruction manual, user's manual and caution labels on the product.
(2) Even within the gratis warranty term, repairs shall be charged for in the following cases.
1. Failure occurring from inappropriate storage or handling, carelessness or negligence by the user. Failure caused by the user's hardware or software design.
2. Failure caused by unapproved modifications, etc., to the product by the user.
3. When the Mitsubishi product is assembled into a user's device, Failure that could have been avoided if functions or structures, judged as necessary in the legal safety measures the user's device is subject to or as necessary by industry standards, had been provided.
4. Failure that could have been avoided if consumable parts (battery, backlight, fuse, etc.) designated in the instruction manual had been correctly serviced or replaced.
5. Failure caused by external irresistible forces such as fires or abnormal voltages, and Failure caused by force majeure such as earthquakes, lightning, wind and water damage.
6. Failure caused by reasons unpredictable by scientific technology standards at time of shipment from Mitsubishi.
7. Any other failure found not to be the responsibility of Mitsubishi or that admitted not to be so by the user.

2. Onerous repair term after discontinuation of production

(1) Mitsubishi shall accept onerous product repairs for seven (7) years after production of the product is discontinued. Discontinuation of production shall be notified with Mitsubishi Technical Bulletins, etc.
(2) Product supply (including repair parts) is not available after production is discontinued.

3. Overseas service

Overseas, repairs shall be accepted by Mitsubishi's local overseas FA Center. Note that the repair conditions at each FA Center may differ.

4. Exclusion of loss in opportunity and secondary loss from warranty liability

Regardless of the gratis warranty term, Mitsubishi shall not be liable for compensation of damages caused by any cause found not to be the responsibility of Mitsubishi, loss in opportunity, lost profits incurred to the user by Failures of Mitsubishi products, special damages and secondary damages whether foreseeable or not , compensation for accidents, and compensation for damages to products other than Mitsubishi products, replacement by the user, maintenance of on-site equipment, start-up test run and other tasks.

5. Changes in product specifications

The specifications given in the catalogs, manuals or technical documents are subject to change without prior notice.

6. Product application

(1) In using the Mitsubishi MELSEC programmable logic controller, the usage conditions shall be that the application will not lead to a major accident even if any problem or fault should occur in the programmable logic controller device, and that backup and fail-safe functions are systematically provided outside of the device for any problem or fault.
(2) The Mitsubishi programmable logic controller has been designed and manufactured for applications in general industries, etc. Thus, applications in which the public could be affected such as in nuclear power plants and other power plants operated by respective power companies, and applications in which a special quality assurance system is required, such as for Railway companies or Public service purposes shall be excluded from the programmable logic controller applications.
In addition, applications in which human life or property that could be greatly affected, such as in aircraft, medical applications, incineration and fuel devices, manned transportation, equipment for recreation and amusement, and safety devices, shall also be excluded from the programmable logic controller range of applications.
However, in certain cases, some applications may be possible, providing the user consults their local Mitsubishi representative outlining the special requirements of the project, and providing that all parties concerned agree to the special circumstances, solely at the users discretion.

Digital-Analog Converter Module
Type A616DAV

User's Manual

MODEL	A616DAV-USERS-E
MODEL CODE	13J650
IB(NA)-66172-C(0411)MEE	

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